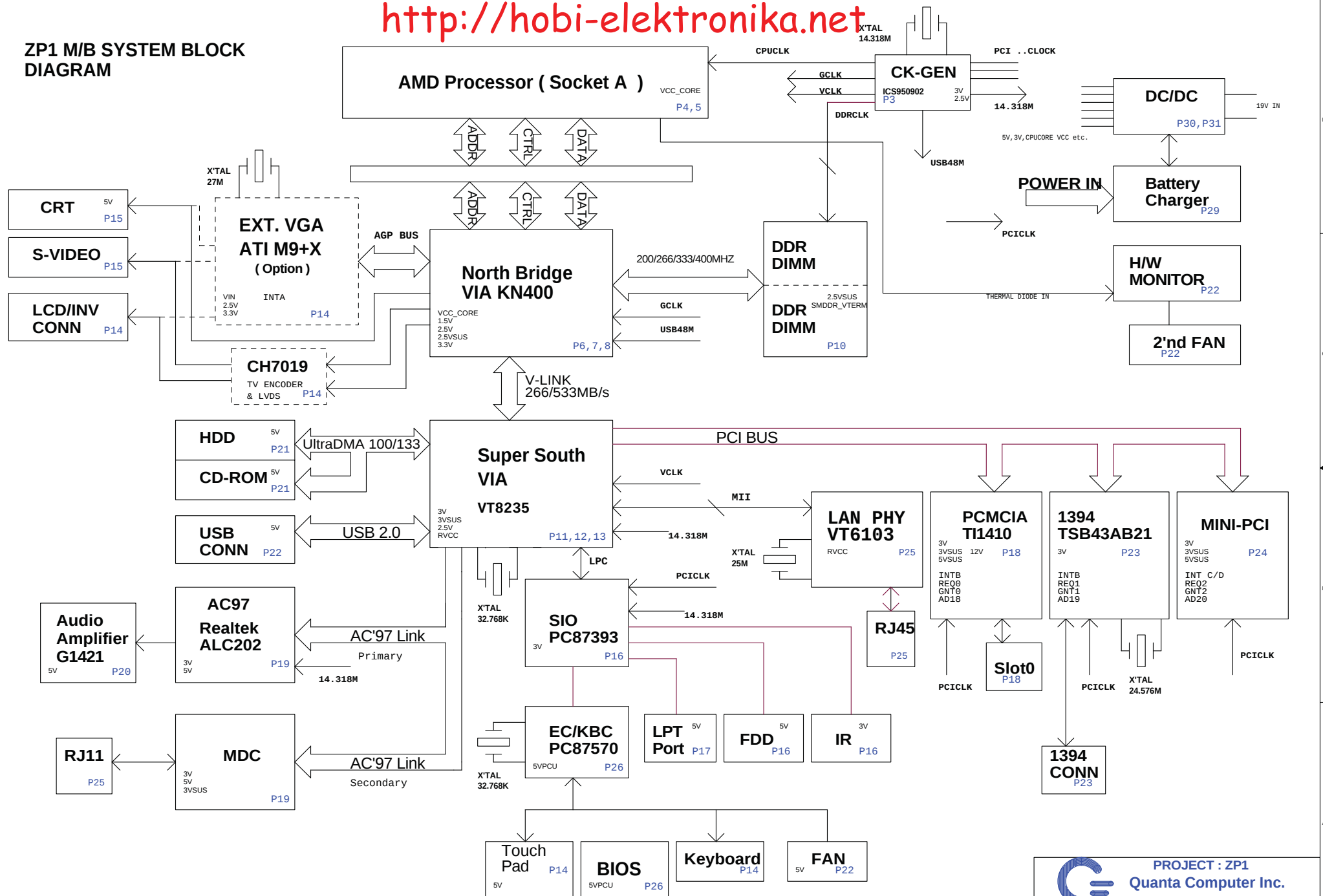




Quanta Computer Inc.

ZP1 M/B SYSTEM BLOCK DIAGRAM



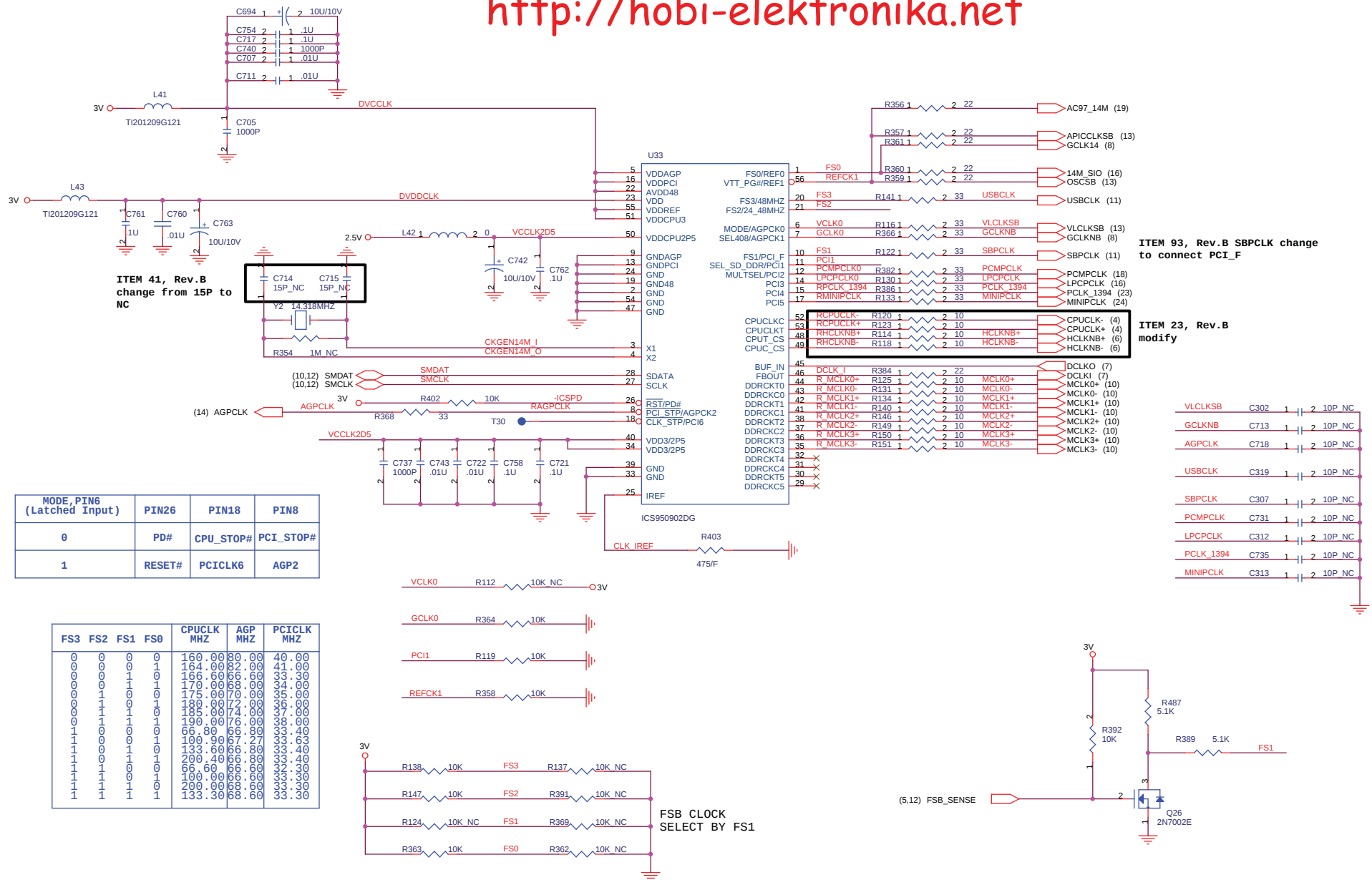
Voltage Rails	Core voltage for Processor	ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC CORE	Core voltage for Processor	X				VR_ON
SMDDR_VTERM	1.25V for DDR Termination voltage	X				MAINON
SMDDR_VREF	1.25V for DDR Reference Voltage	X				MAINON
1.5V		X				MAINON
2.5VSUS		X	X			SUSON
2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
5V		X				MAINON
12V		X				MAINON
12VOUT		X	X	X	X	VL
RVCC		X	X	X		RVCC_ON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ/GNT#	Interrupts
CB1410	AD18	-REQ0/-GNT0	INTB
TSB43AB21	AD19	-REQ1/-GNT1	INTB
MINI-PCI	AD20	-REQ2/-GNT2	INT C/D
AGP			INTA



PROJECT : ZP1
Quanta Computer Inc.

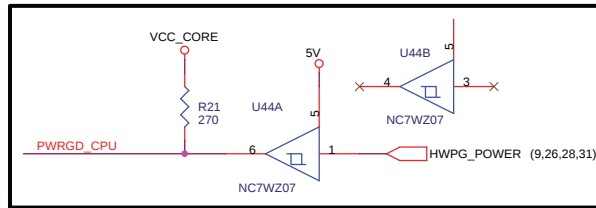
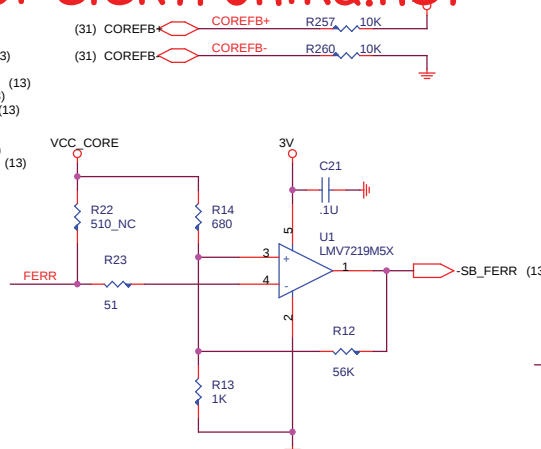
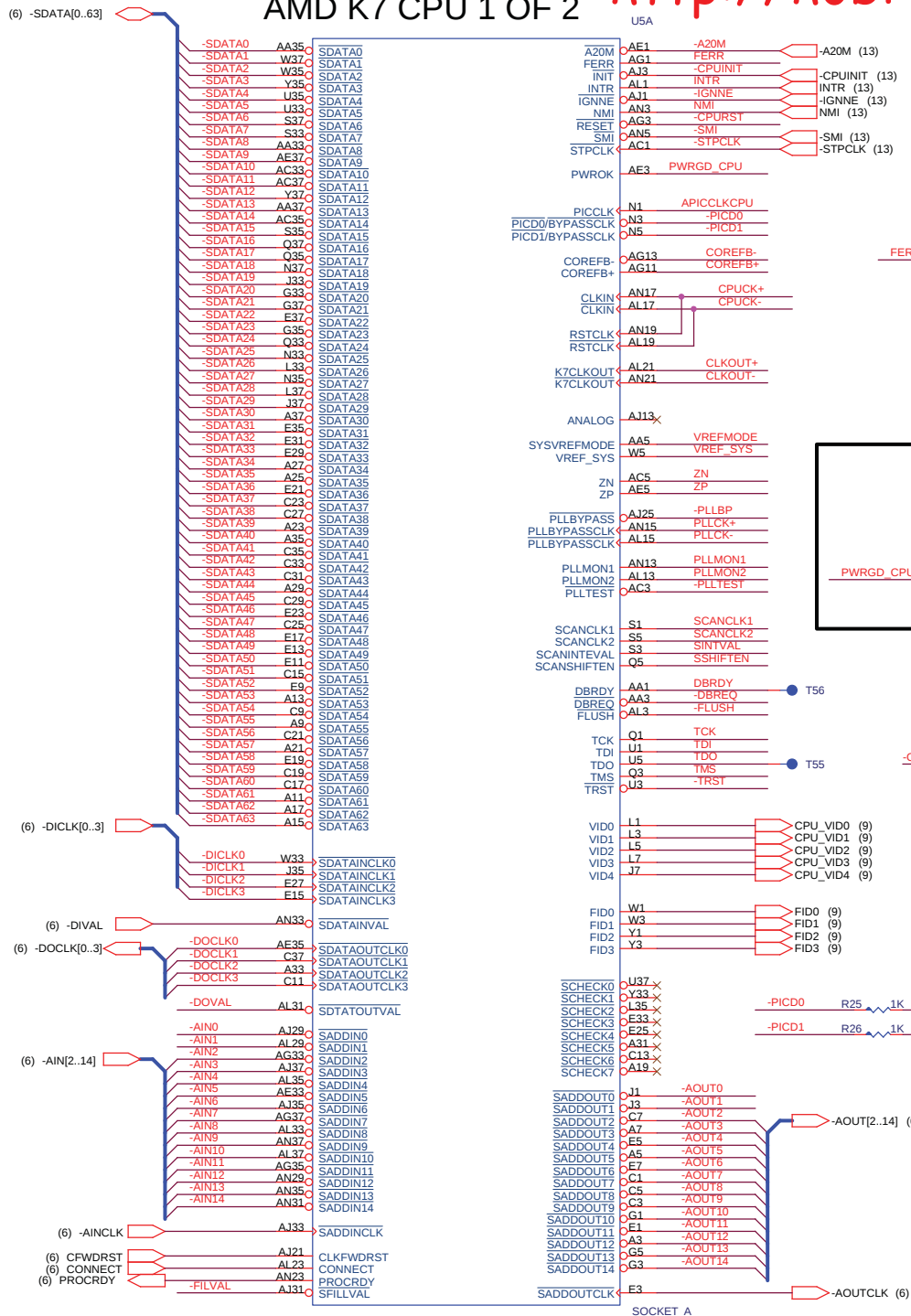
Size A4	Document Number	Rev 1A
INFORMATION		
Date:	Wednesday, September 17, 2003	Sheet 2 of 32



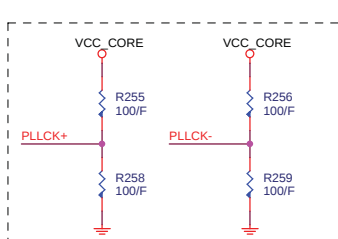
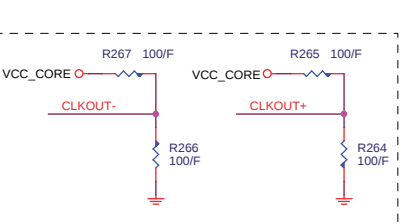
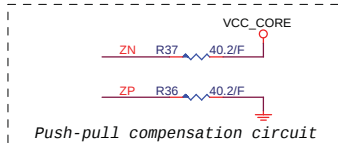
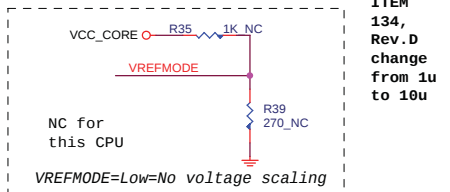
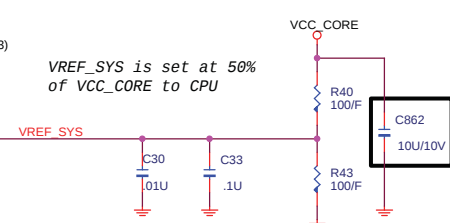
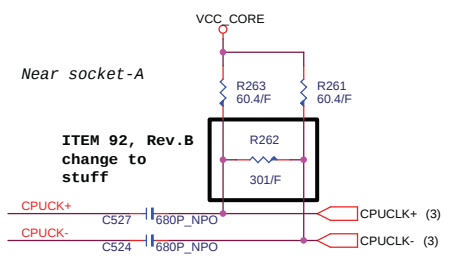
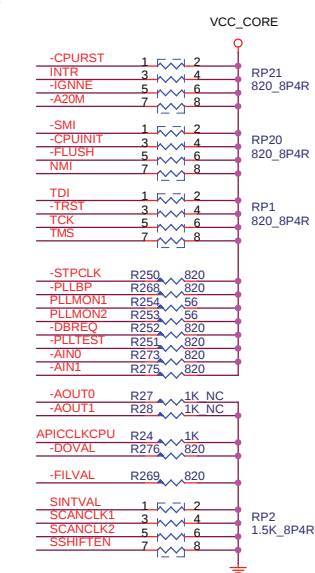
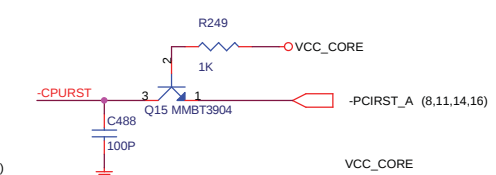
CPU FSB SENSE TABLE		CLKGEN SETTING				CPU CLK
FSB_SENSE		FS3	FS2	FS1	FS0	
0		1	1	1	1	133MHZ
1		1	1	0	1	100MHZ

FS3/48MHZ : INTERNAL 120K PULL-UP RESISTOR TO VDD
 FS2/24_48MHZ : INTERNAL 120K PULL-UP RESISTOR TO VDD
 FS1/PCI_F : INTERNAL 120K PULL-DOWN RESISTOR TO GND
 FS0/REF0 : INTERNAL 120K PULL-UP RESISTOR TO VDD

AMD K7 CPU 1 OF 2



ITEM 30, Rev.B modify this circuit



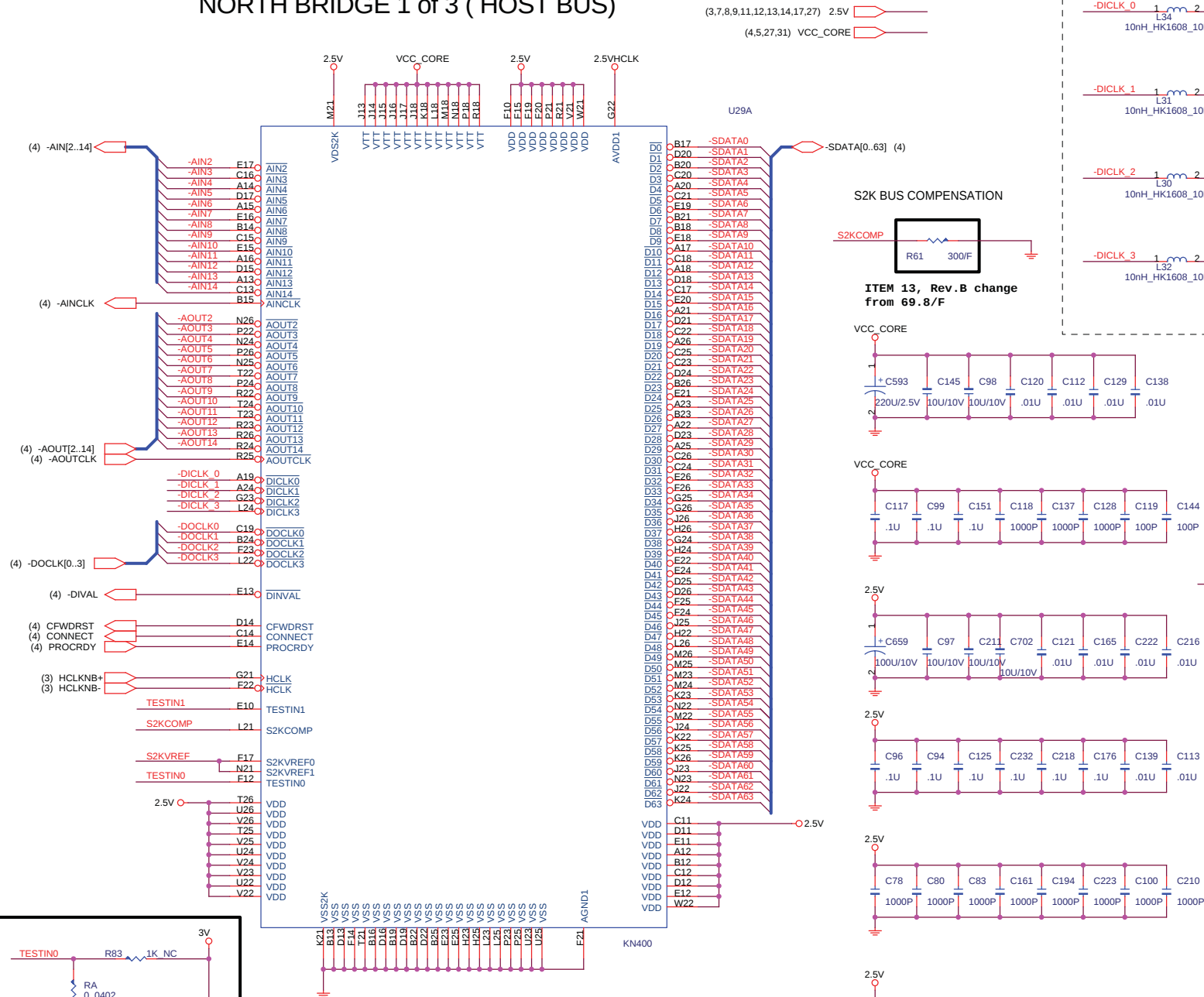


PROJECT : ZP1

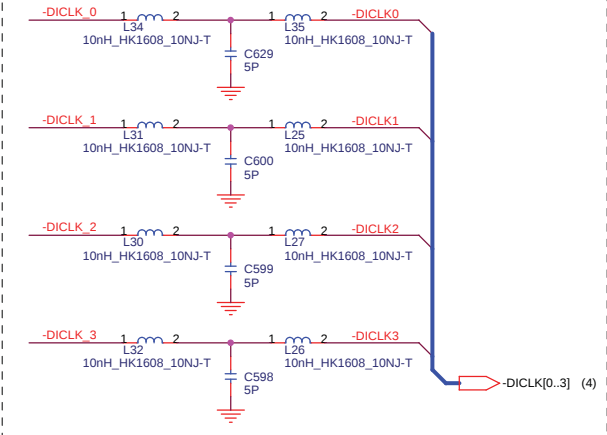
Quanta Computer Inc.

Size C	Document Number	CPU-1(S2K)	Rev 3A
Date:	Wednesday, September 17, 2003	Sheet	4 of 32

NORTH BRIDGE 1 of 3 (HOST BUS)



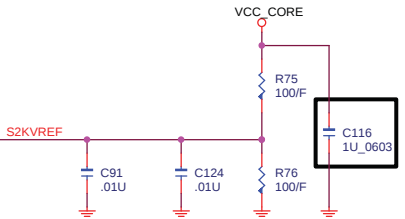
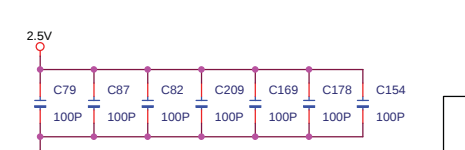
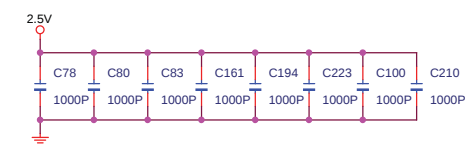
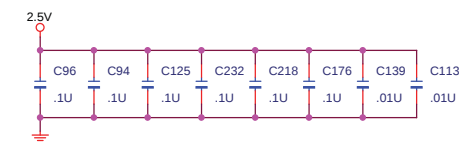
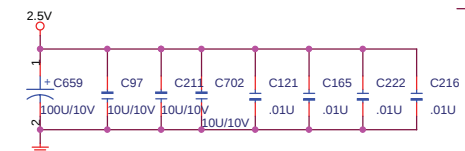
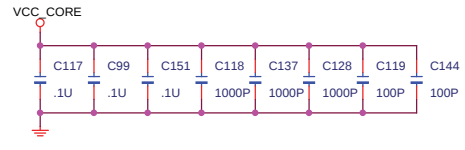
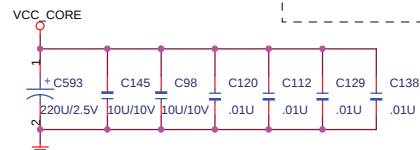
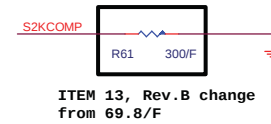
LCL FILTER



PLACED NEAR NORTH BRIDGE

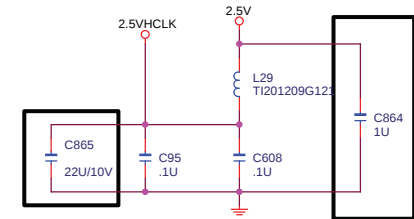
NORTH BRIDGE S2K REFERENCE
VOTAGE (1/2 VCC_CORE)
PLACED UNDER BGA

S2K BUS COMPENSATION

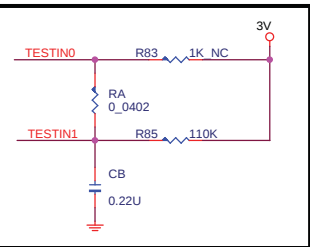


ITEM 75, Rev.B
change from
0.1U

AVDDHCLK/AGNDHCLK : POWER/GROUND FOR
INTERNAL CPU CLOCK LOGIC

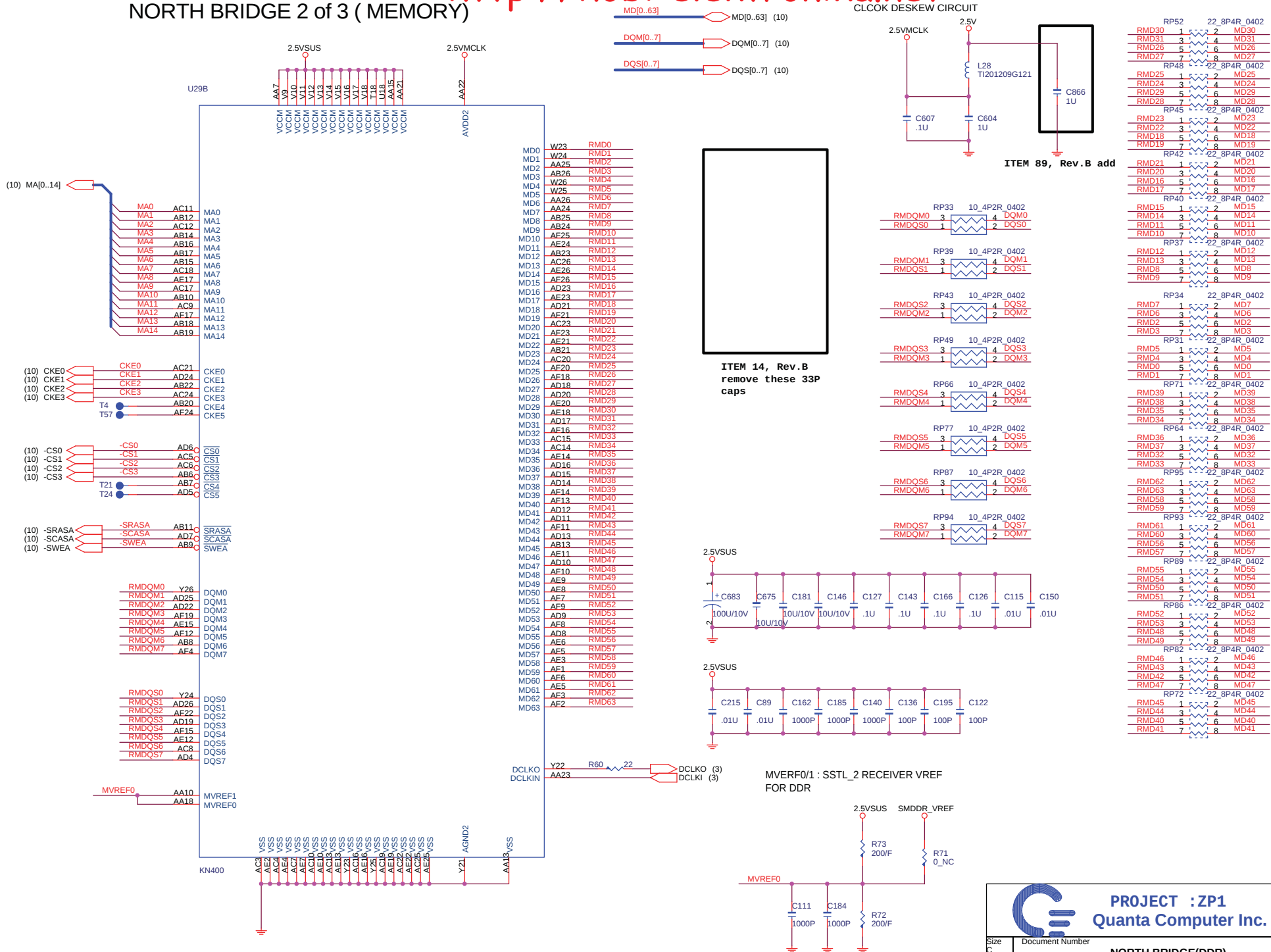


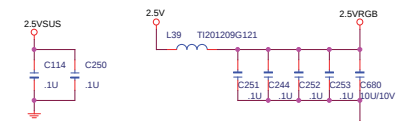
ITEM 89, Rev.B add



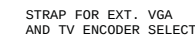
ITEM 196, Rev.E3H
rework

NORTH BRIDGE 2 of 3 (MEMORY)





ITEM 106, Rev.B2B R328 change from 1K to 4.7K

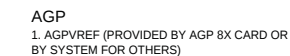


VCC5
3.3V FOR PANEL I/F LOGIC



PLACE CLOSE TO N/B

1. VLINK REFERENCE VOLTAGE 0.9V

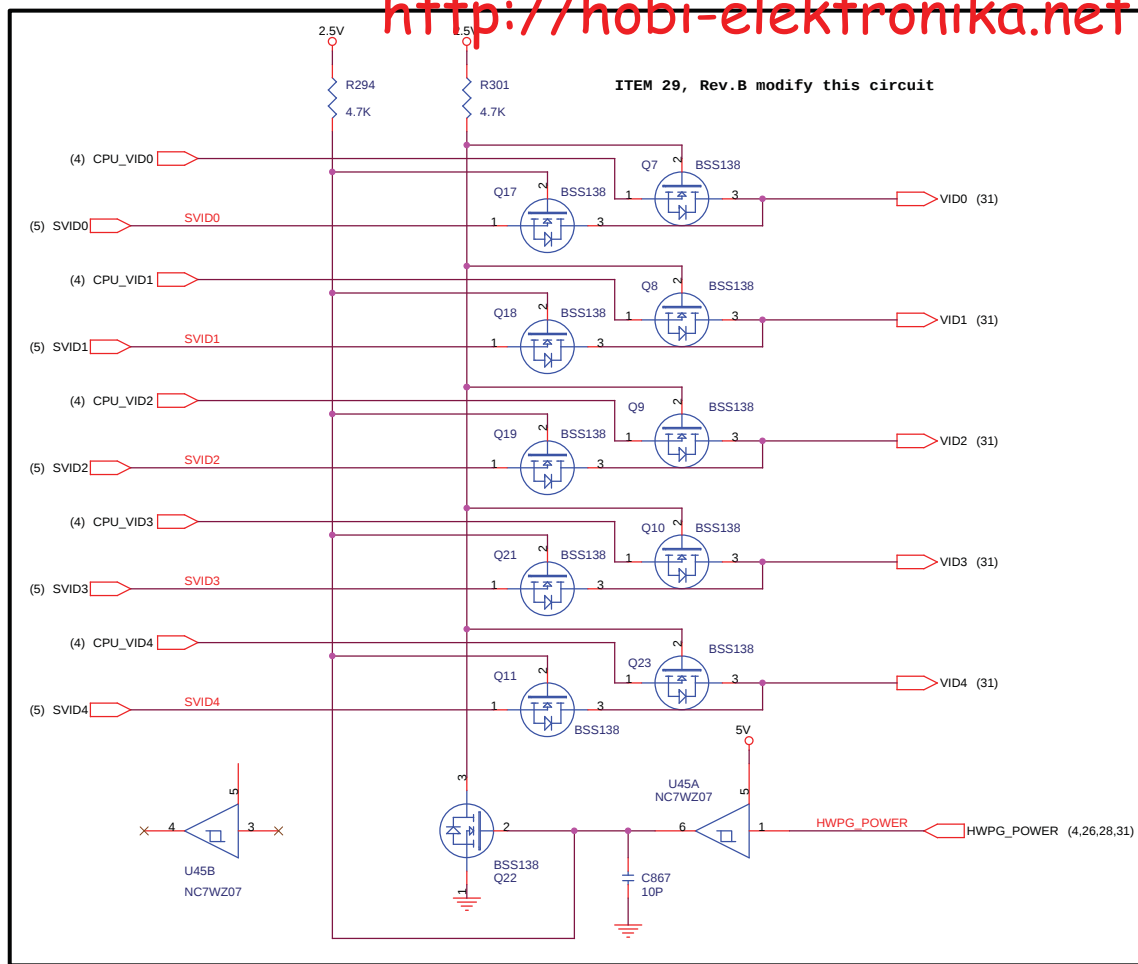
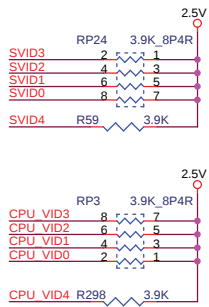


COMPENSATION

2.5V NORTH BRIDGE VCORE



AMD suggest 3.9K



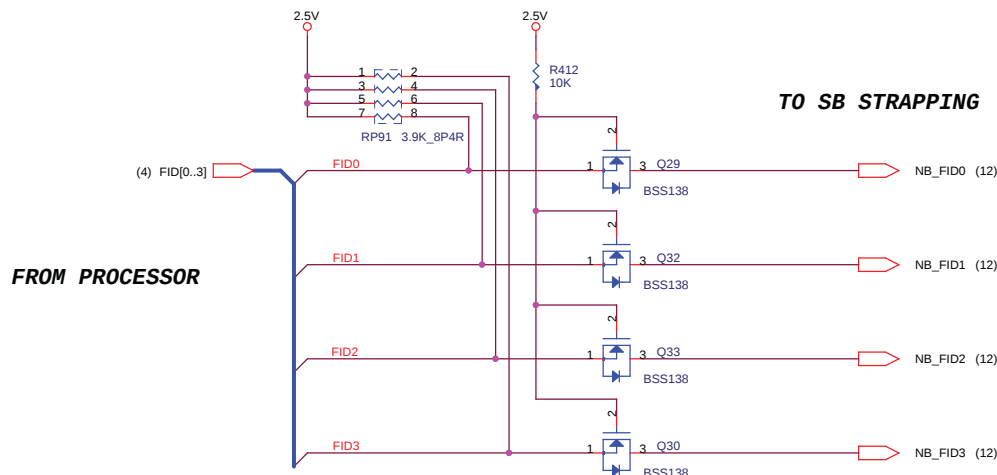
VID / FID Interface

VID Codes

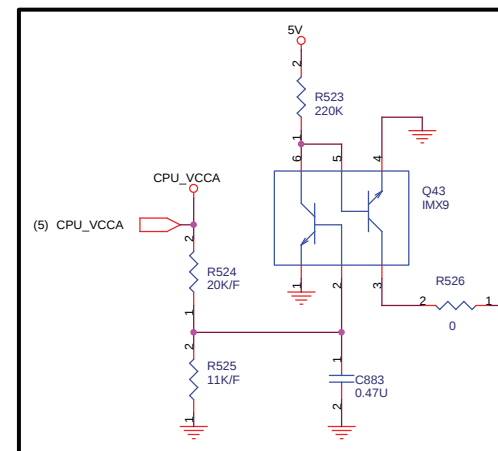
VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	SHUTDOWN	11111	SHUTDOWN

FID Codes

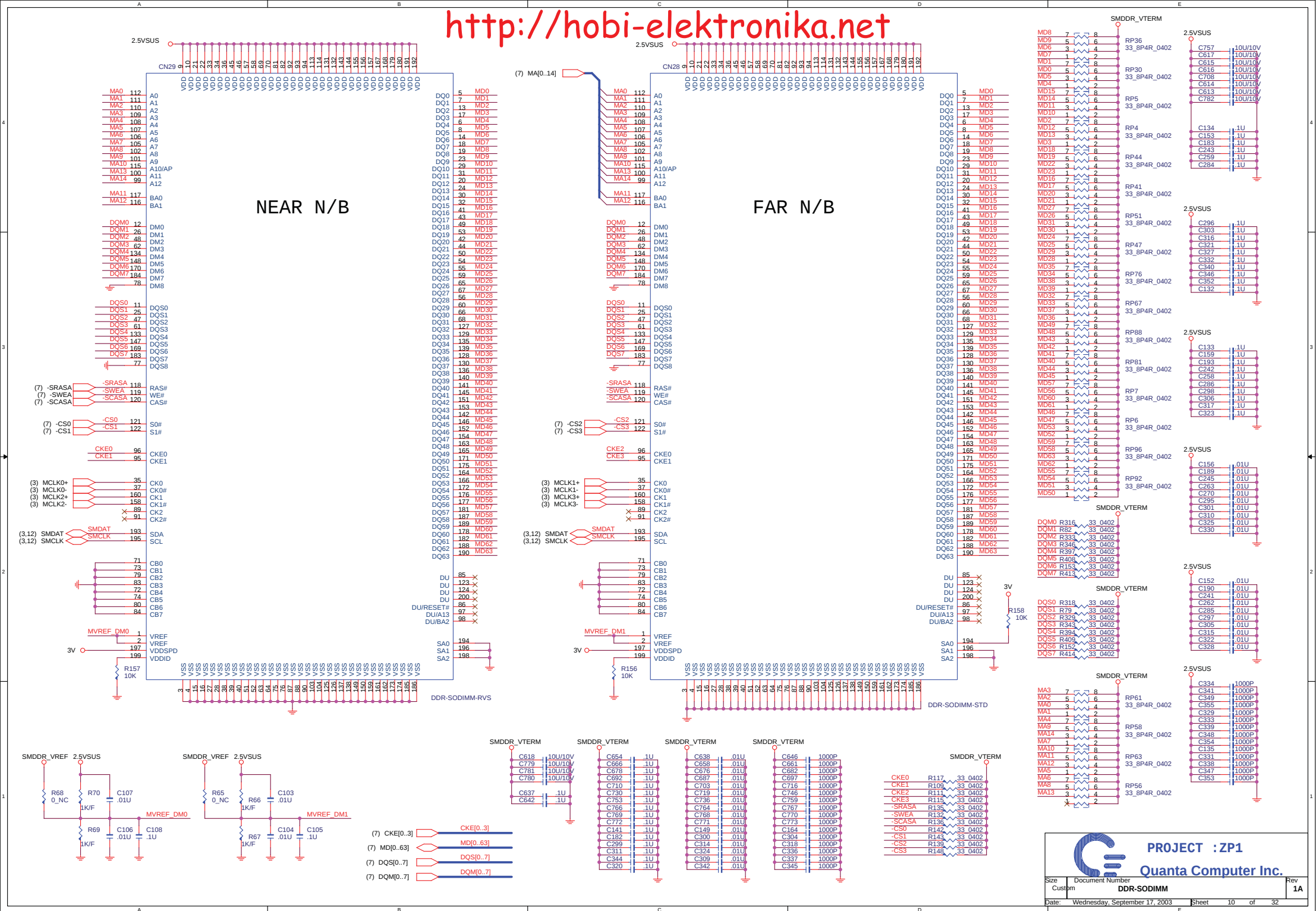
Four-Bit FID	Clock Multiplier	Four-Bit FID	Clock Multiplier
0000	11.0	1000	7.0
0001	11.5	1001	7.5
0010	12.0	1010	8.0
0011	12.5	1011	8.5
0100	5.0	1100	9.0
0101	5.5	1101	9.5
0110	6.0	1110	10.0
0111	6.5	1111	10.5



TO SB STRAPPING



ITEM 131, Rev.D add



ITEM 160, Rev.D change
from 3V to 3VSUS

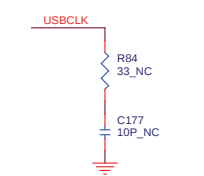
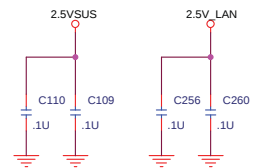
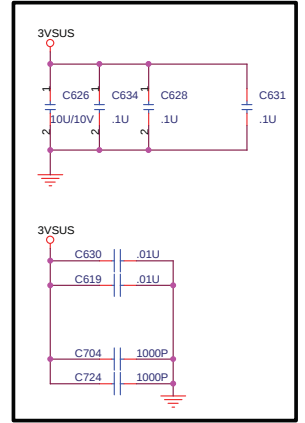
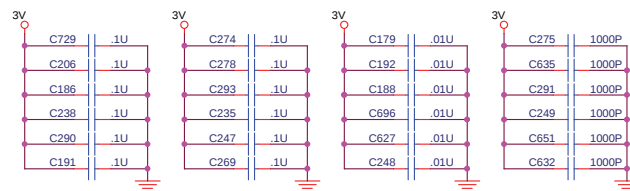
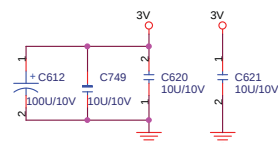
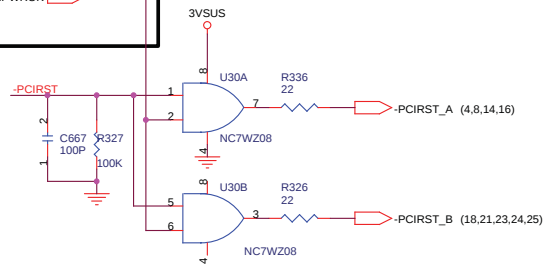
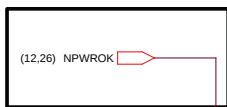
ITEM 167,
Rev.E change
from 3V to
3VSUS

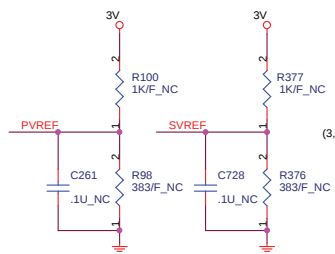
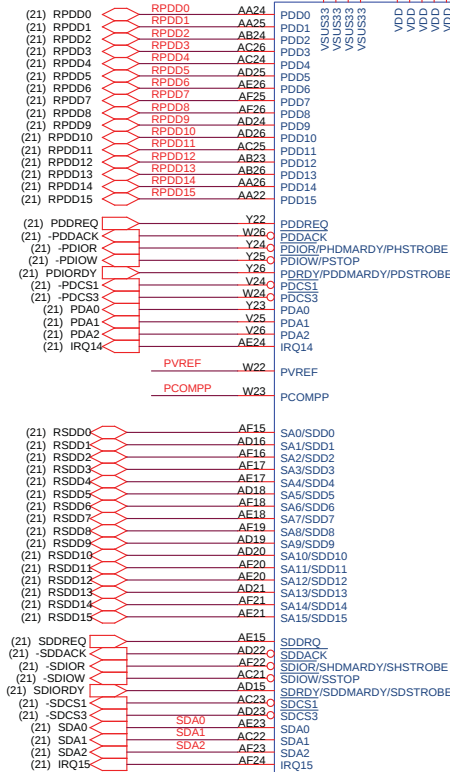
ITEM 103,
Rev.C change
from 2.5V to
2.5VSUS

ITEM 69 Rev.B
bead change
to 0ohm for
EMI.

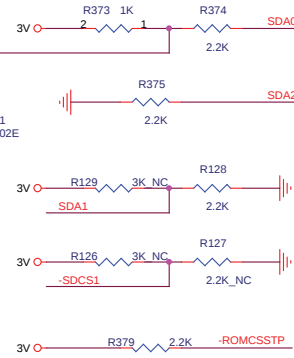
ITEM 146, Rev.D
change from 3V to
3VSUS and add
R529, R530

ITEM 90, Rev.B modify





(3,



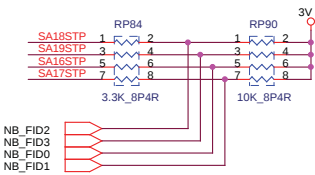
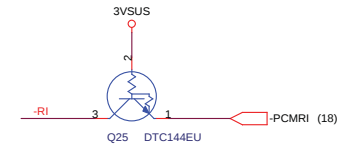
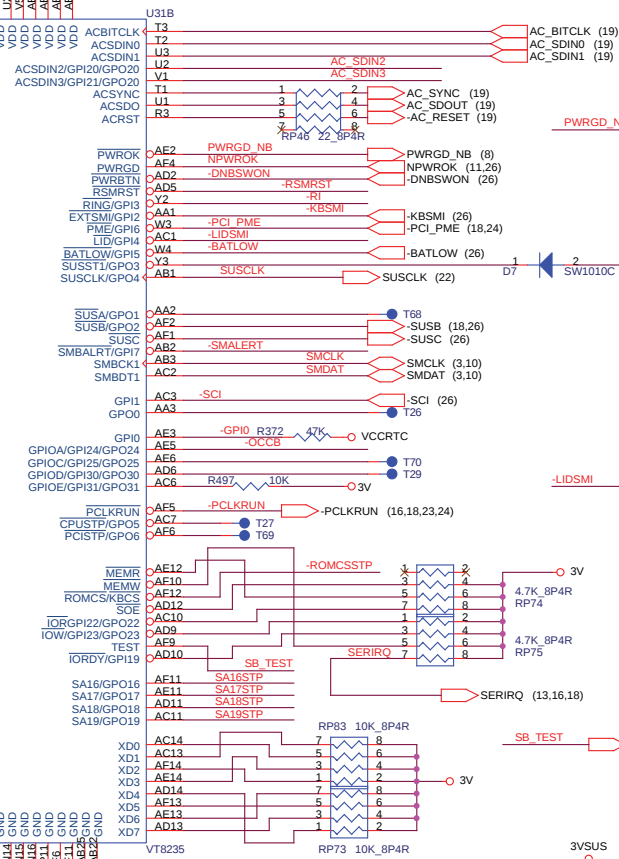
SDA0 => CPU Clock Frequency
 0 - 100MHz (Default)
 1 - 133MHz

SDA2 => CPU Clock Frequency
 0 - strapped by SDA0
 1 - 166MHz

SDA1 => Strapping Information Select
 0 - From Hardware Strapping (Default)
 1 - From Boot ROM

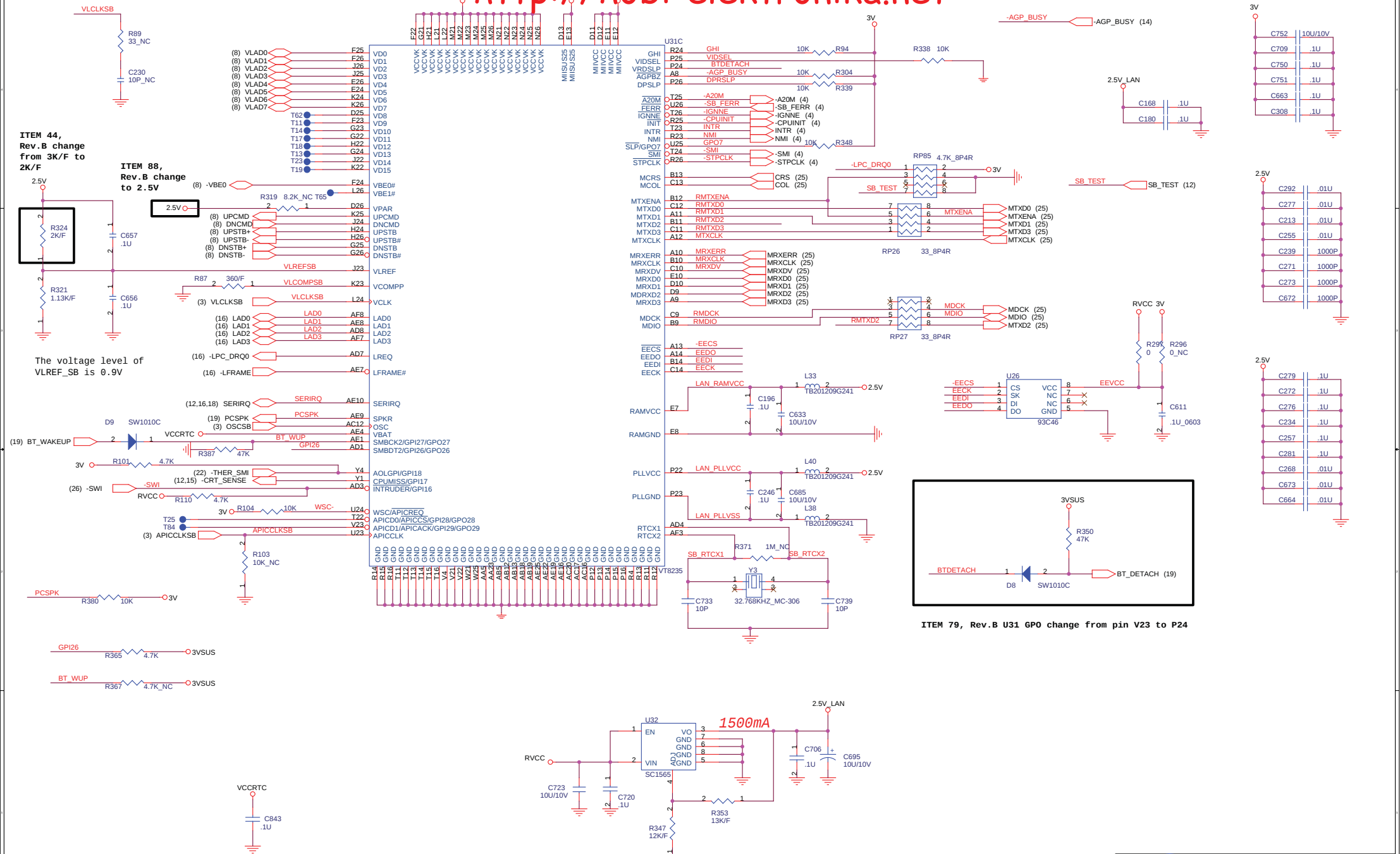
```
-SDCS1 => EEPROM Select
0 - LAN EEPROM interface via the MII bus
1 - LAN EEPROM interface via the EExx pins(internal P/U)
```

```
-ROMCS => LPC ROM Select
0 - Disable LPC BIOS ROM
1 - Enable LPC BIOS ROM
```

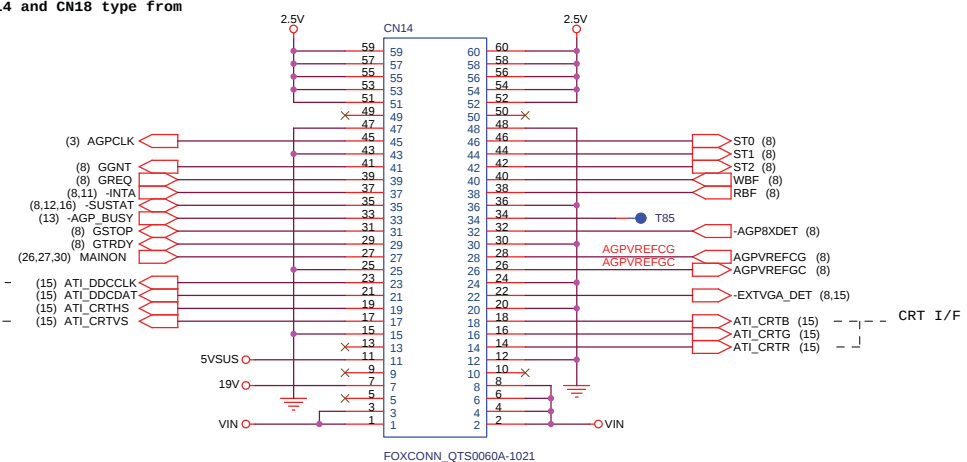
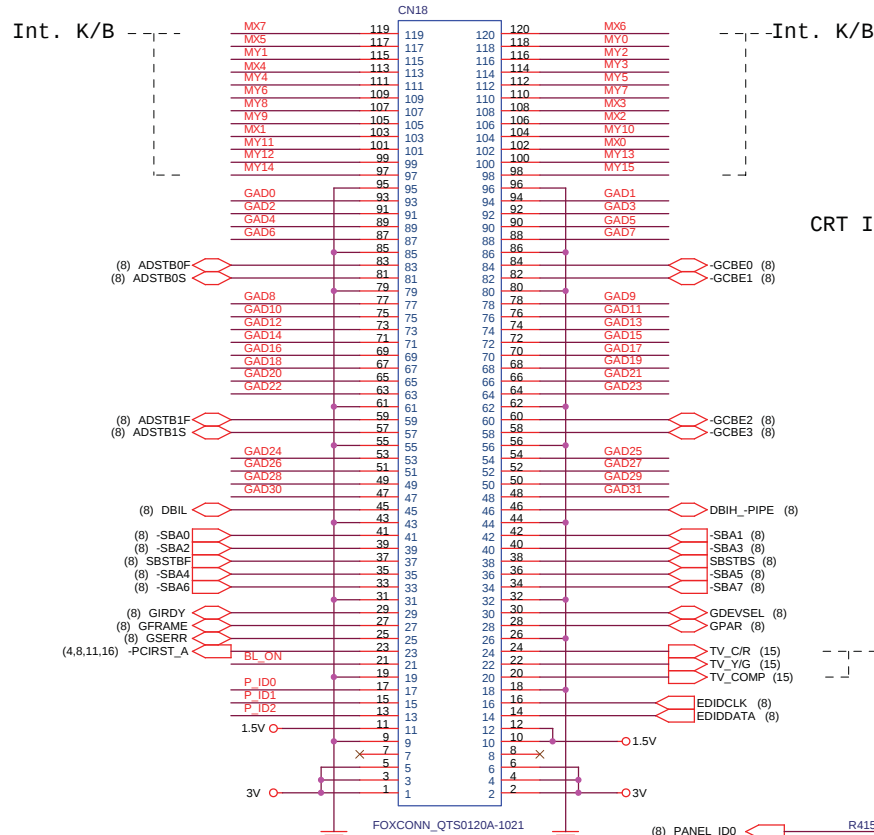


Power Up Strappings :

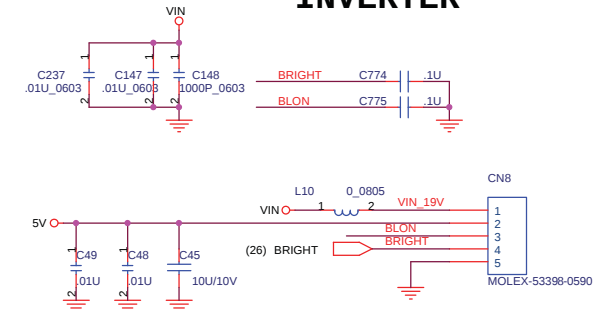
SA[19:16] =>	CPU	Clock	Divider
0000	11	1000	7
0001	11.5	1001	7.5
0010	12	1010	8
0011	12.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	10.5



ITEM 82, Rev.B change CN14 and CN18 type from E & T to Foxconn



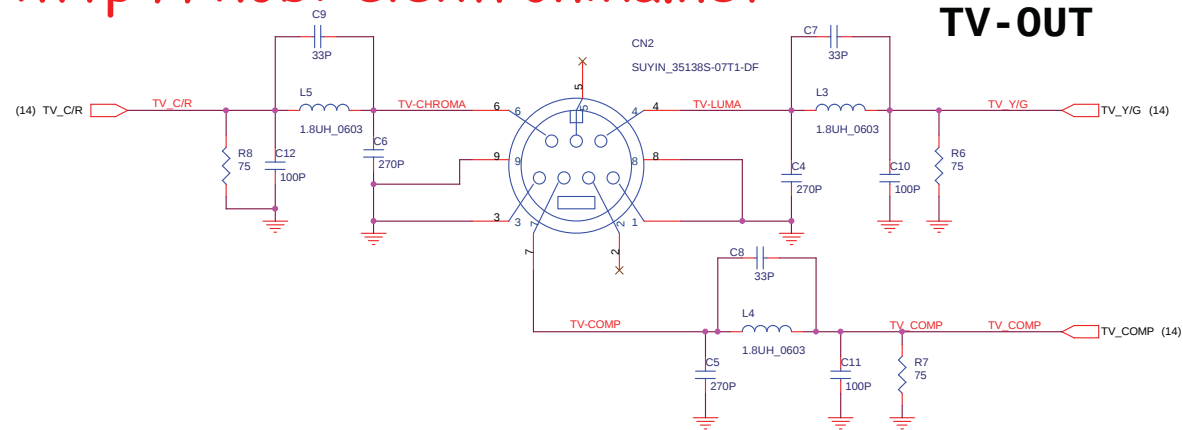
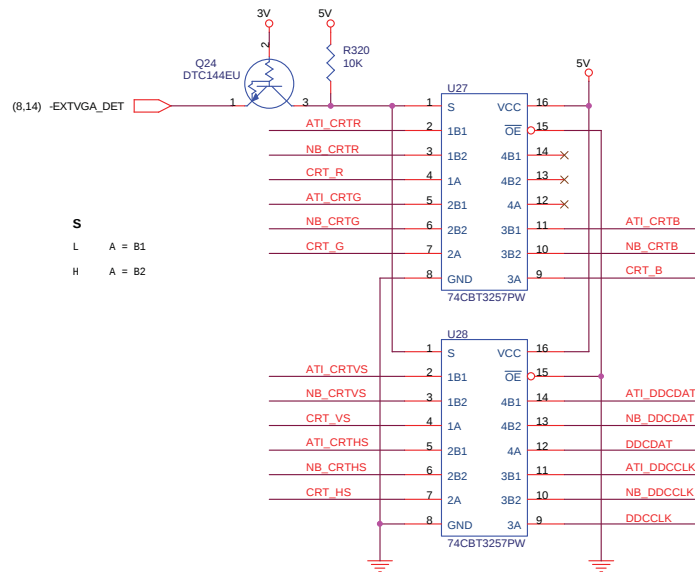
INVERTER



PROJECT : ZP1

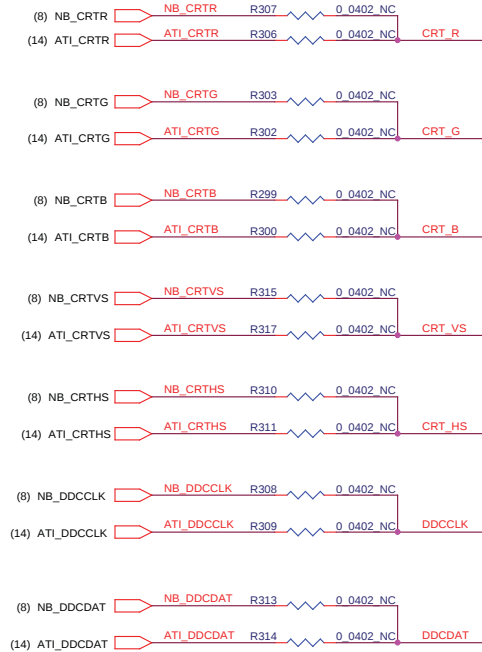
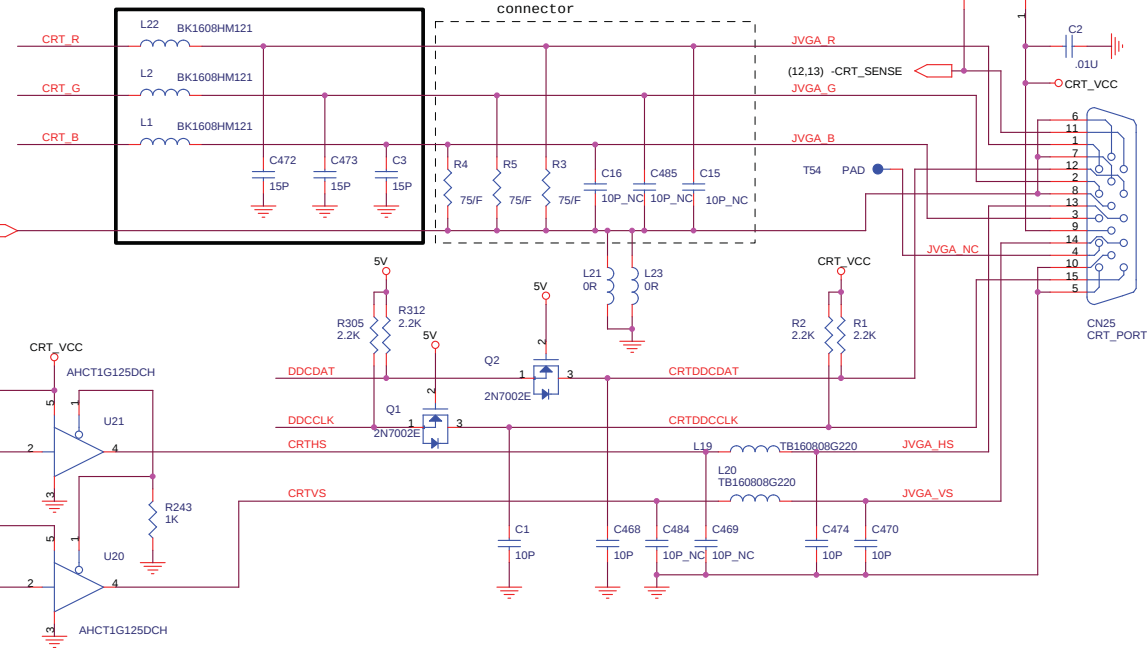
Quanta Computer Inc.

TV-OUT



CRT PORT

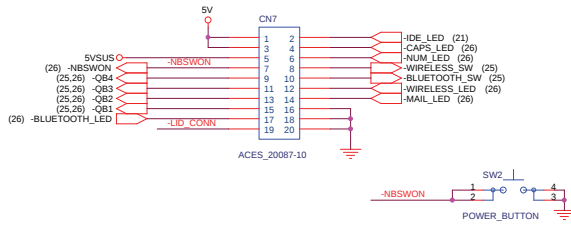
ITEM 65 Rev.B change value and placed near U27 for EMI.





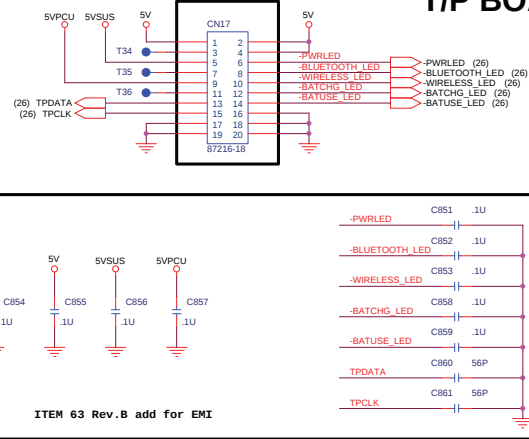
Quanta Computer Inc.

LED BOARD



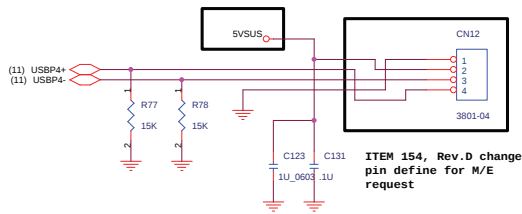
T/P BOARD

ITEM 172, Rev.E change from 18
pin to 20 pin

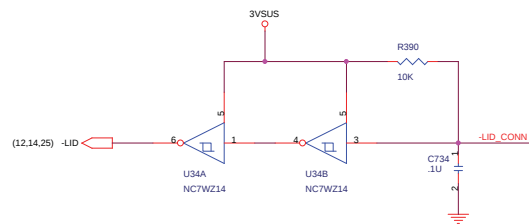


4 IN 1 CARD READER

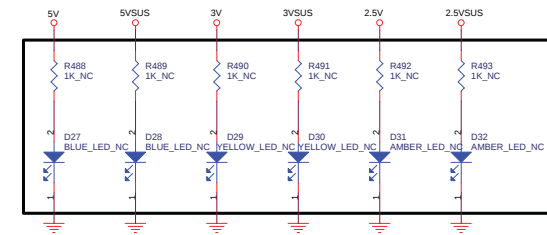
ITEM 175, Rev.E change from 5V to 5VSUS



LID SWITCH



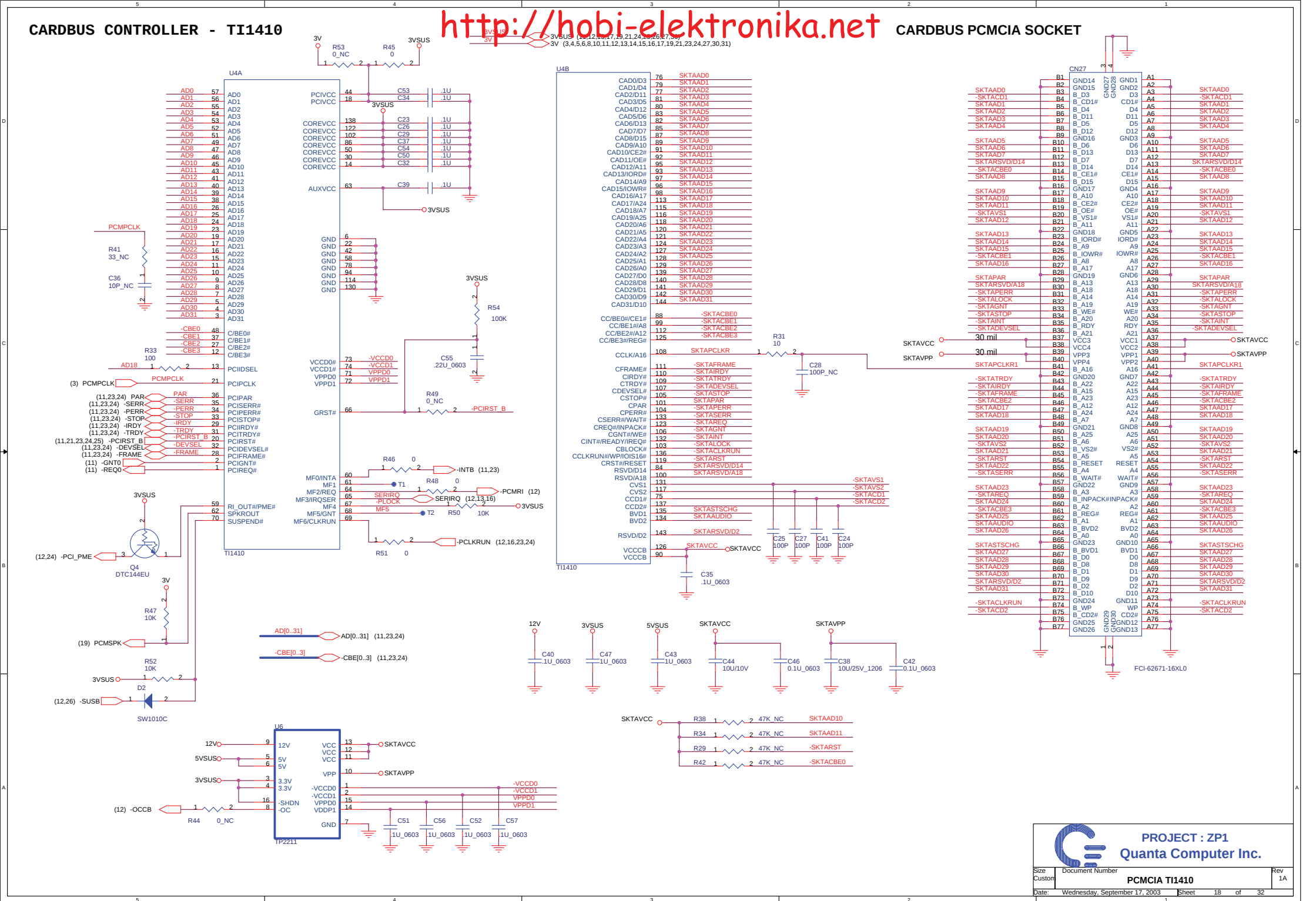
DEBUG LED

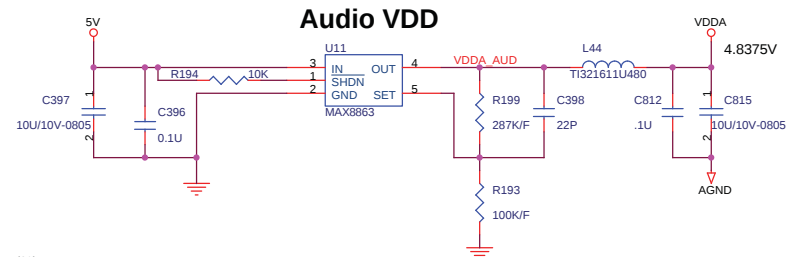
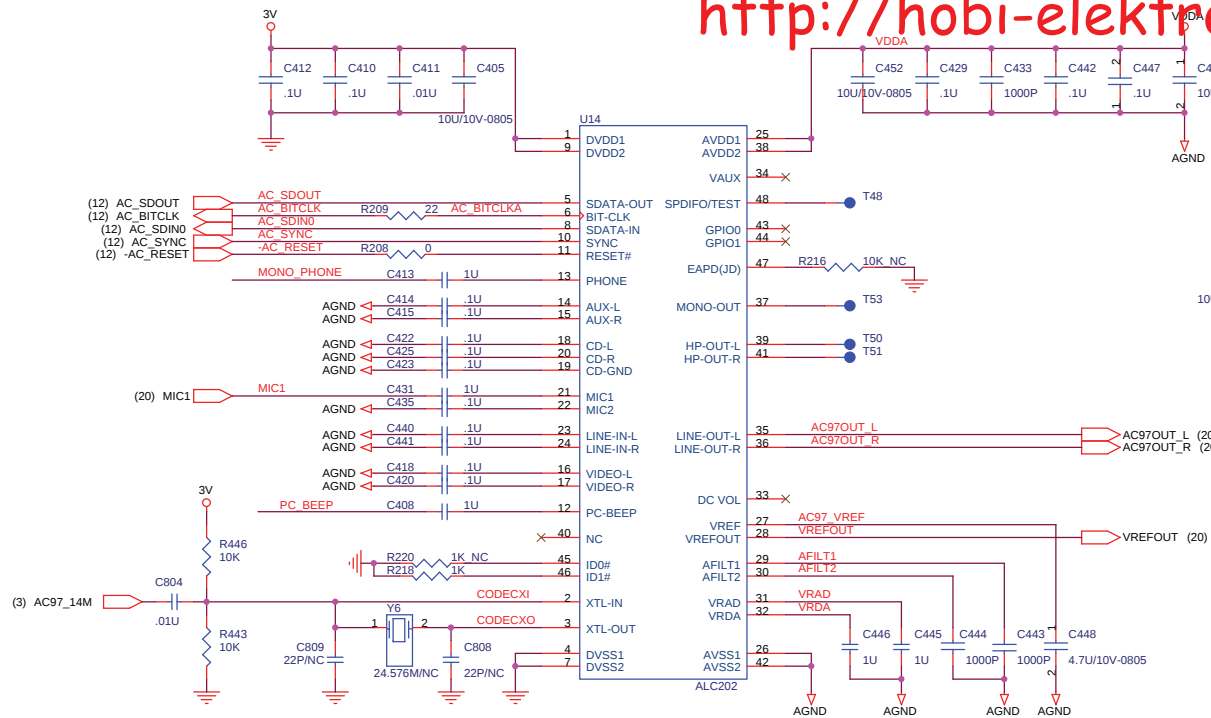


ITEM 97, Rev.C Remove

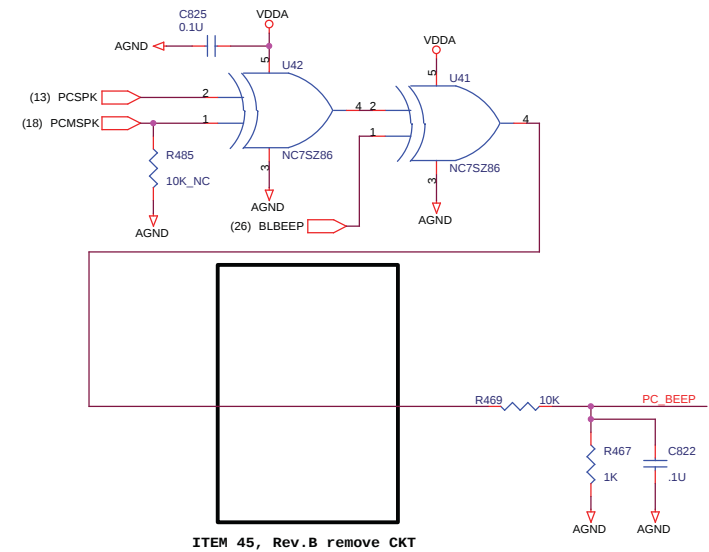
http://hobi-elektronika.net

Size	Document Number			Rev
Custom	PCMCIA TI1410			1A
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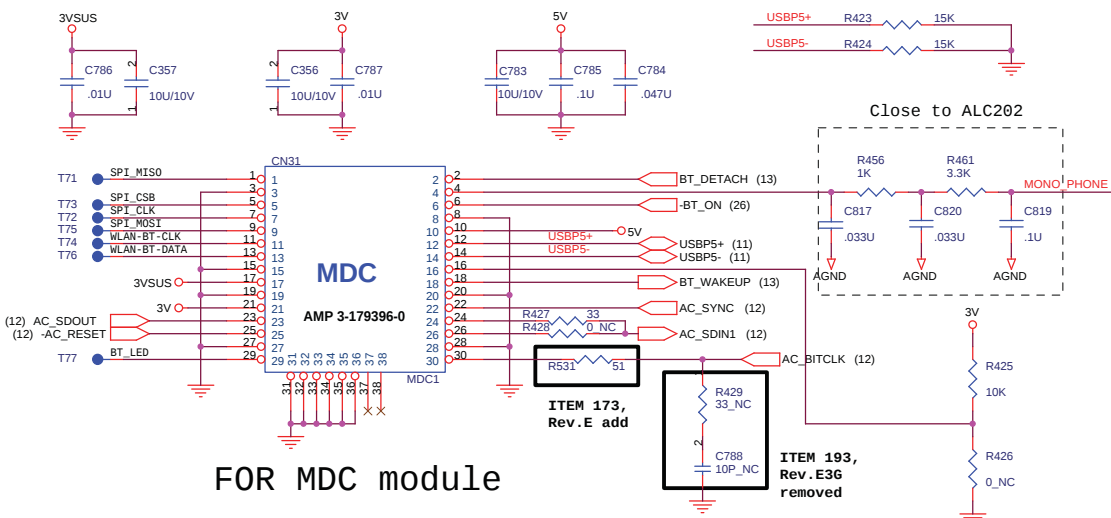




PC SPEAKER



ITEM 45, Rev.B remove CKT



FOR MDC module

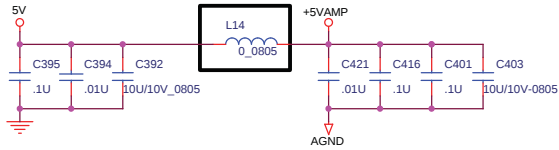
ITEM 173, Rev.E add

ITEM 193, Rev.E36 removed



PROJECT : ZP1
Quanta Computer Inc.

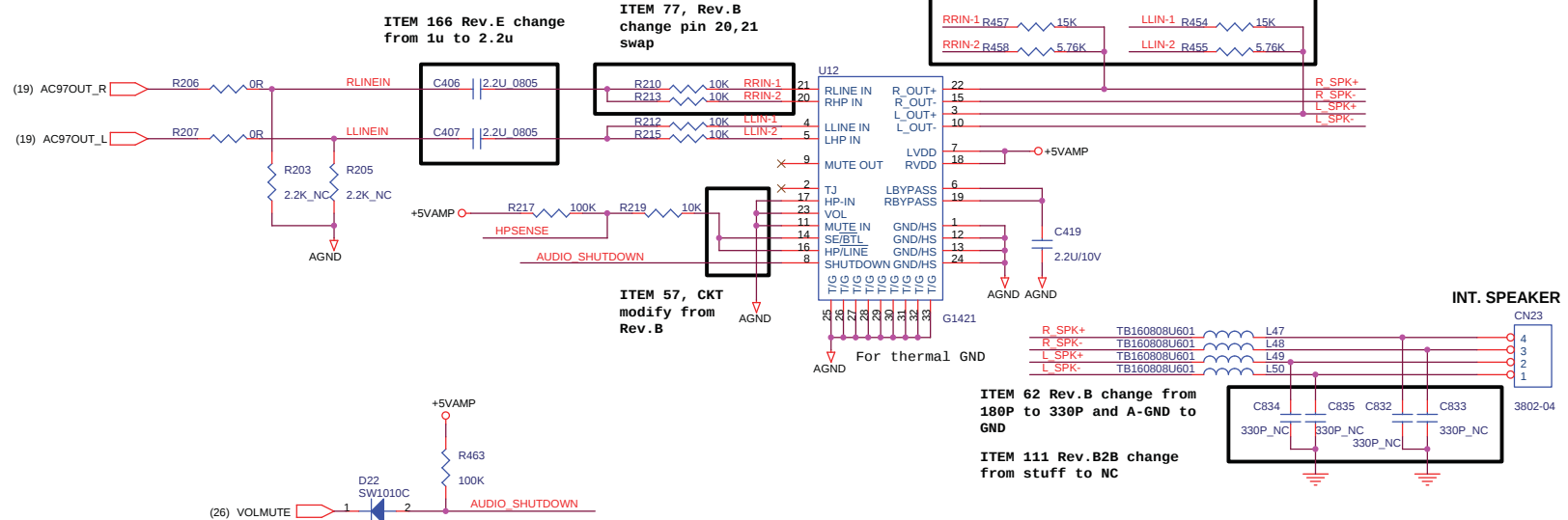
ITEM 69 Rev.B bead
change to 0ohm for EMI.



Audio amplifier

ITEM 81, Rev.B modify

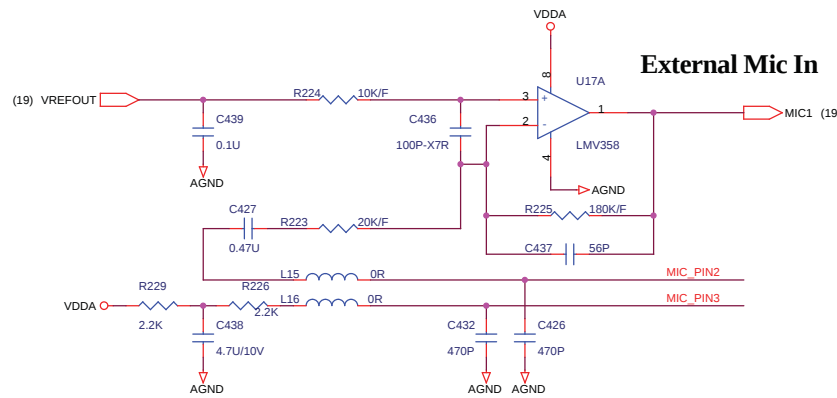
ITEM 111, Rev.B2B change R454,R457 from 24.9K to 15K



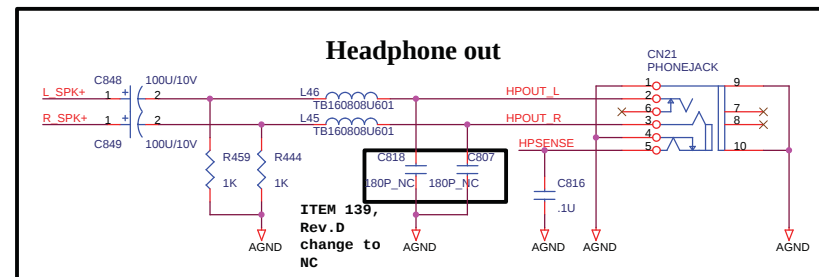
ITEM 62 Rev.B change from
180P to 330P and A-GND to
GND

ITEM 111 Rev.B2B change
from stuff to NC

External Mic In

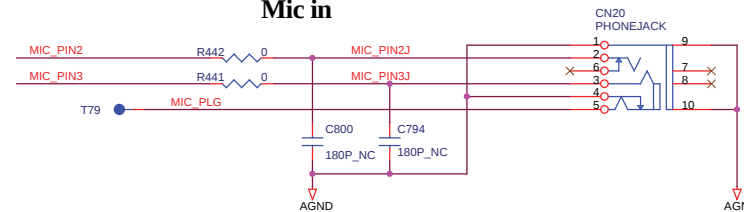


Headphone out



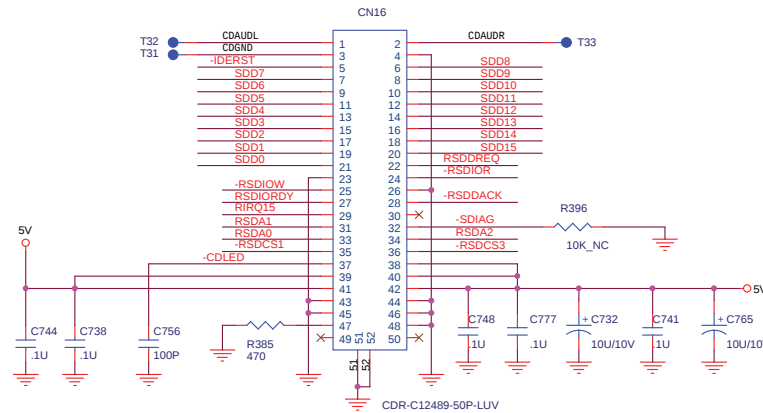
ITEM 57, CKT modify from Rev.B

Mic in

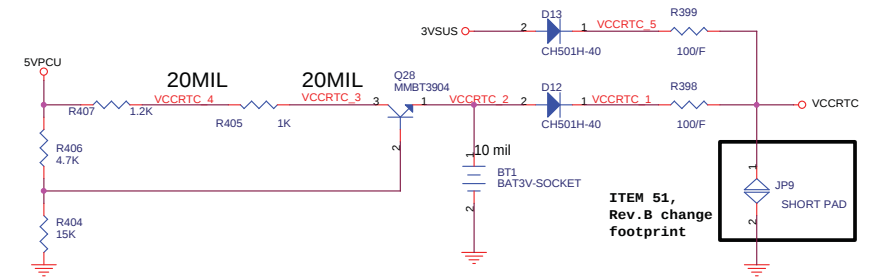


PROJECT : ZP1
Quanta Computer Inc.

ODD CONNECTOR

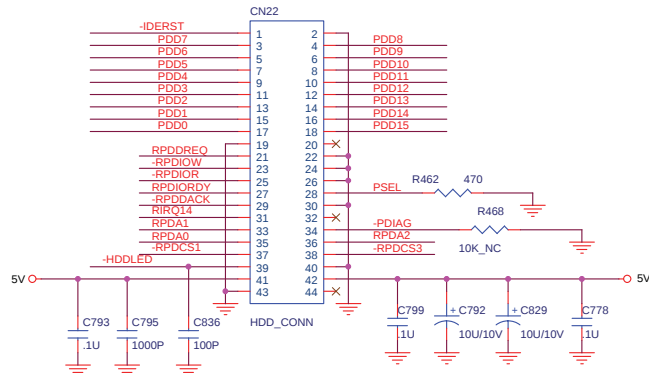
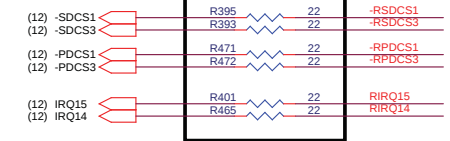


RTC

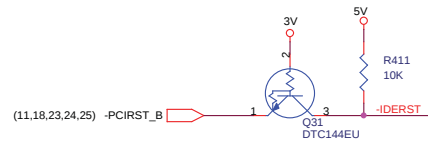
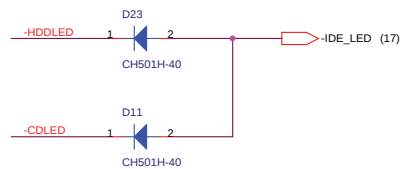


ITEM 51, Rev.B change footprint

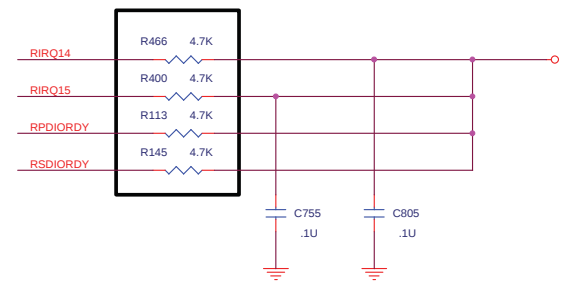
ITEM 38, Rev.B modify, placed near South Bridge



HDD connector



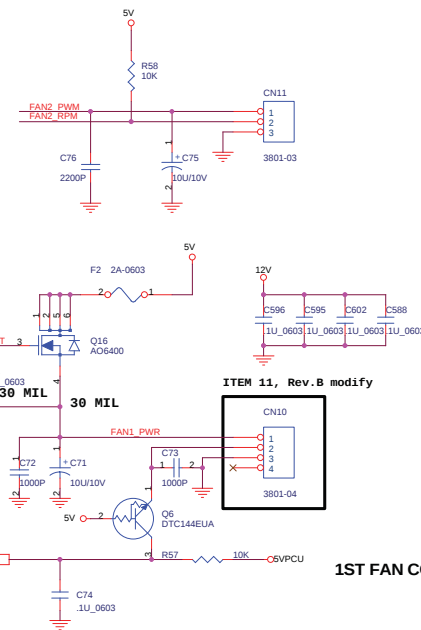
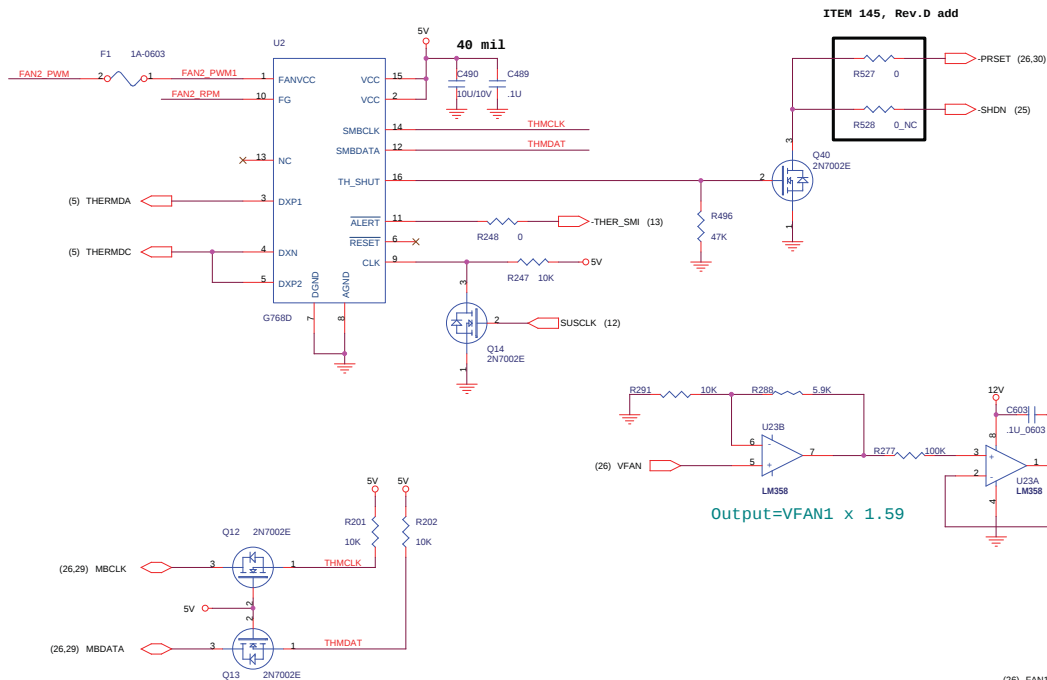
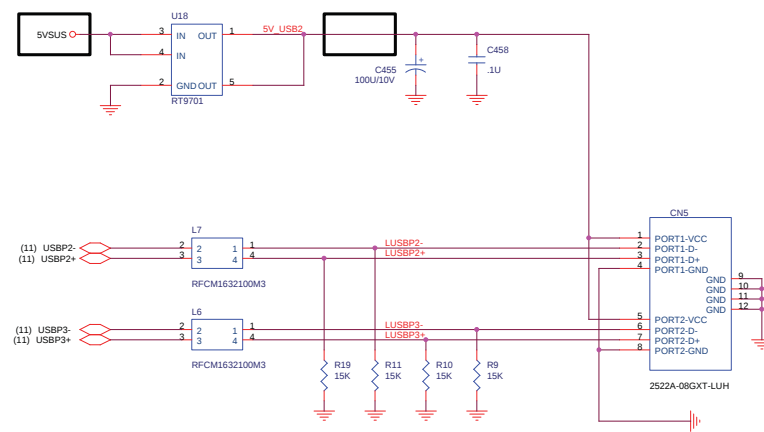
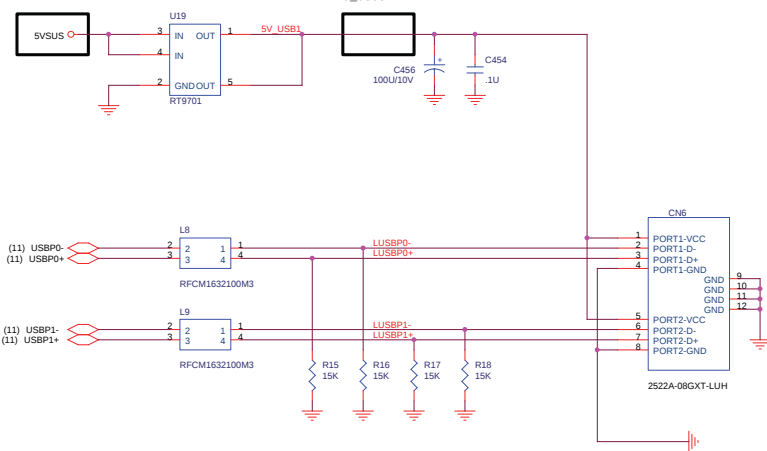
Placed near VT8235



ITEM 35, Rev.B modify, placed near South Bridge



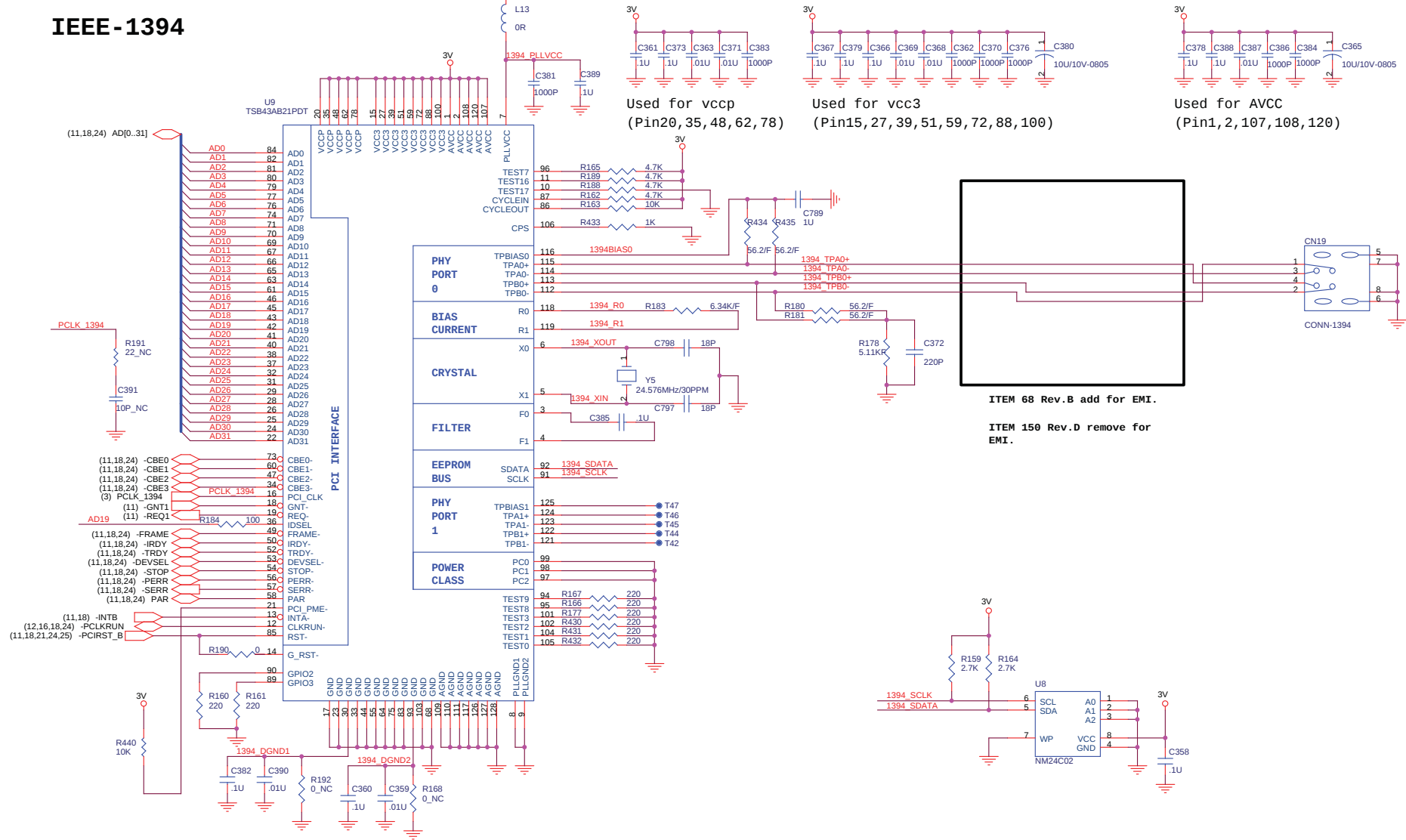
ITEM 36, Rev.B modify, placed near South Bridge



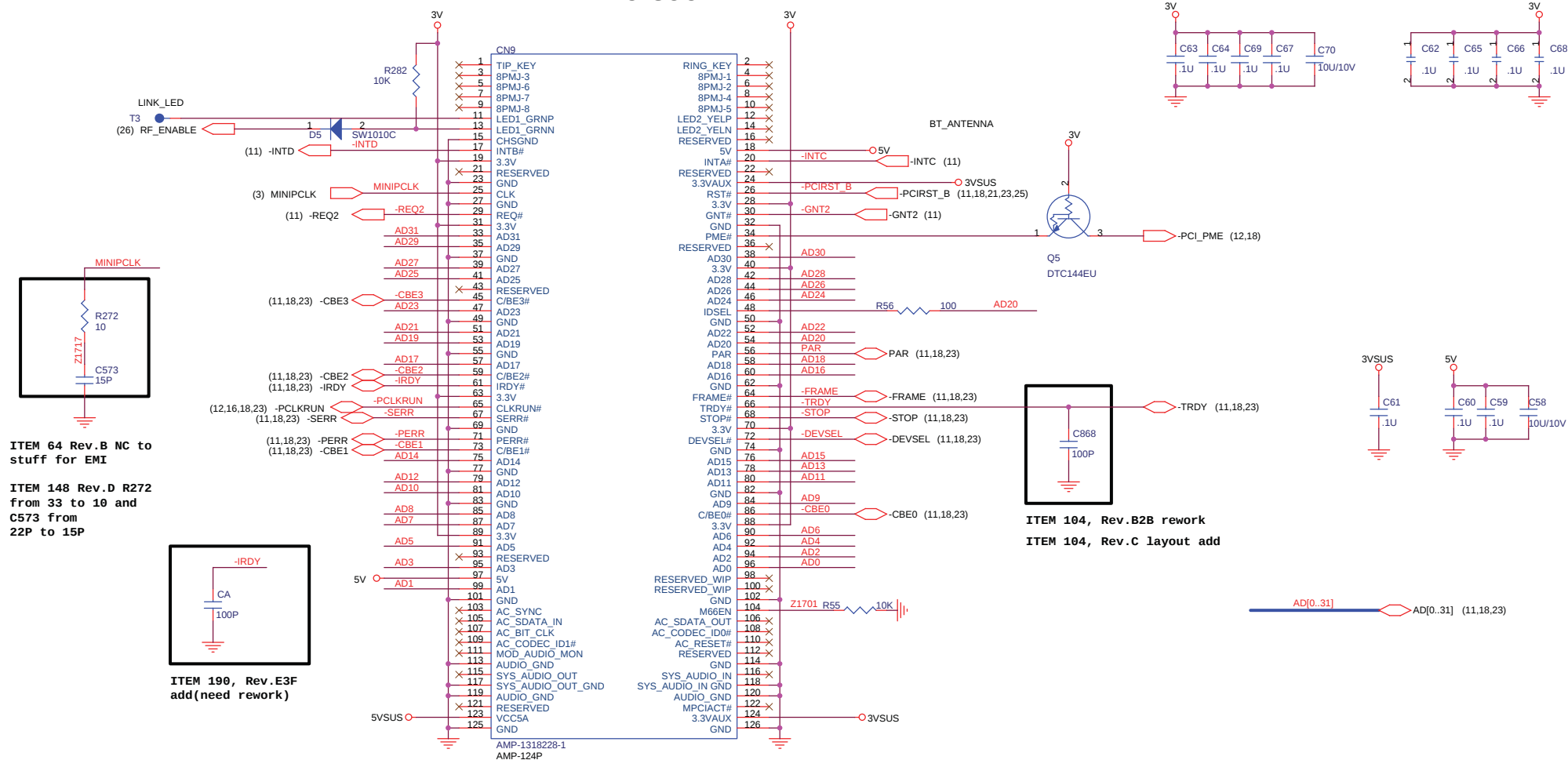
ITEM 146, Rev.D remove
over current event to
system

 PROJECT : ZP1 Quanta Computer Inc.	
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IEEE-1394



TYPE III MINI PCI SOCKET

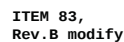
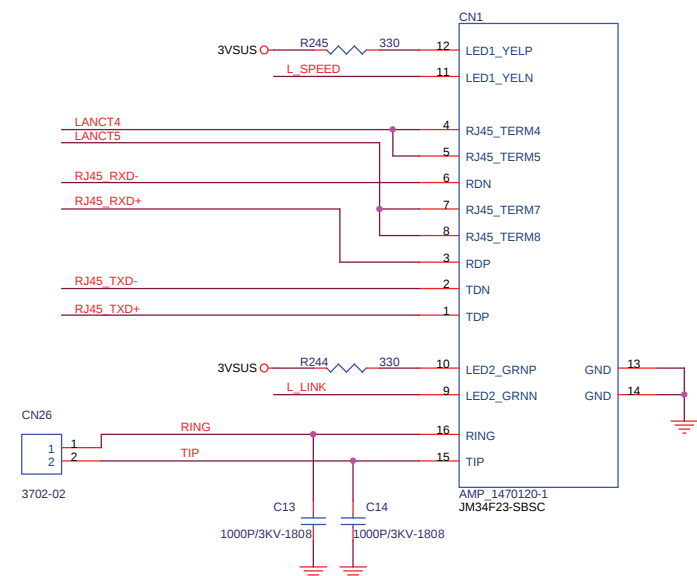
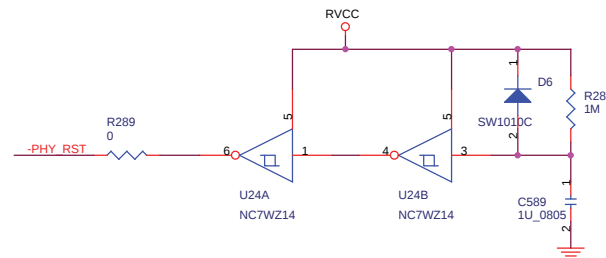
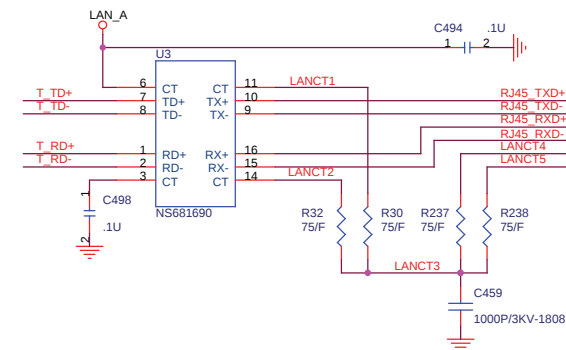


ITEM 64 Rev.B NC to stuff for EMI

ITEM 148 Rev.D R272 from 33 to 10 and C573 from 22P to 15P

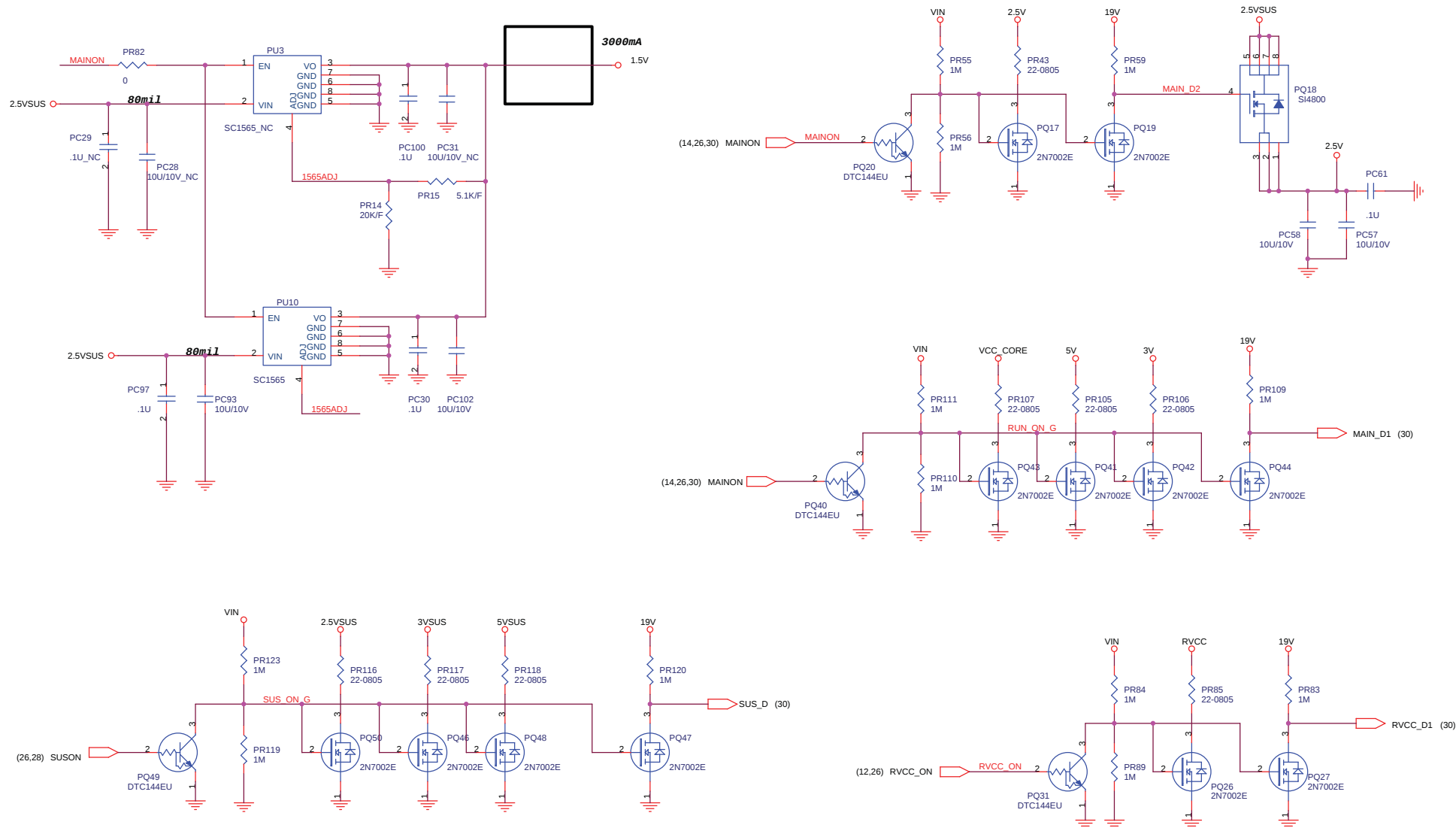
ITEM 190, Rev.E3F add(need rework)

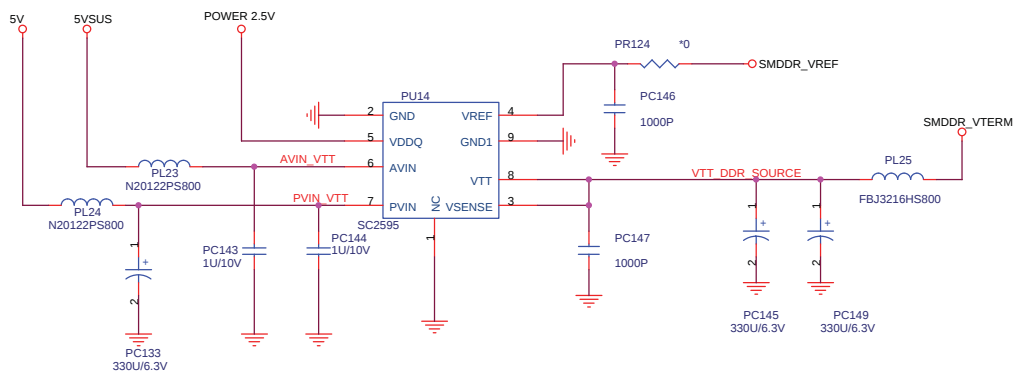
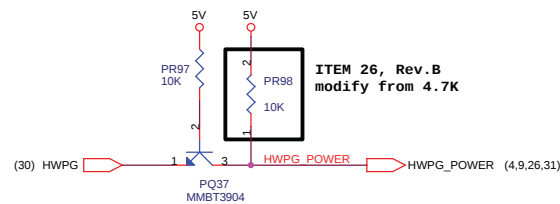
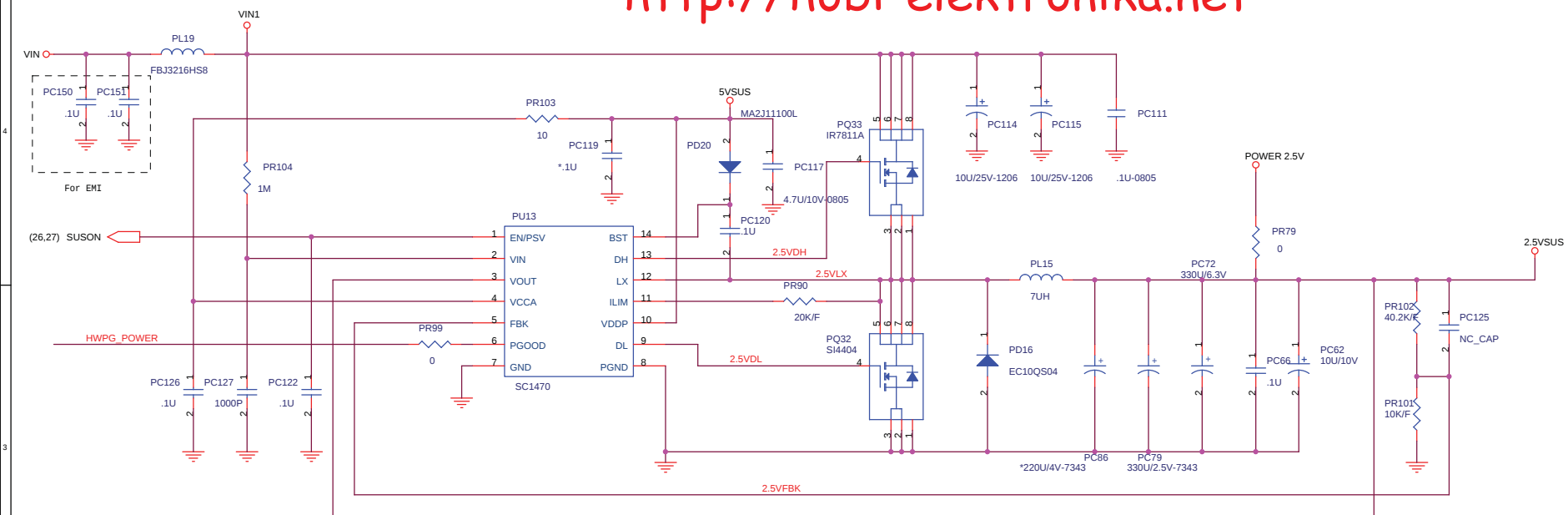
ITEM 104, Rev.B2B rework
ITEM 104, Rev.C layout add

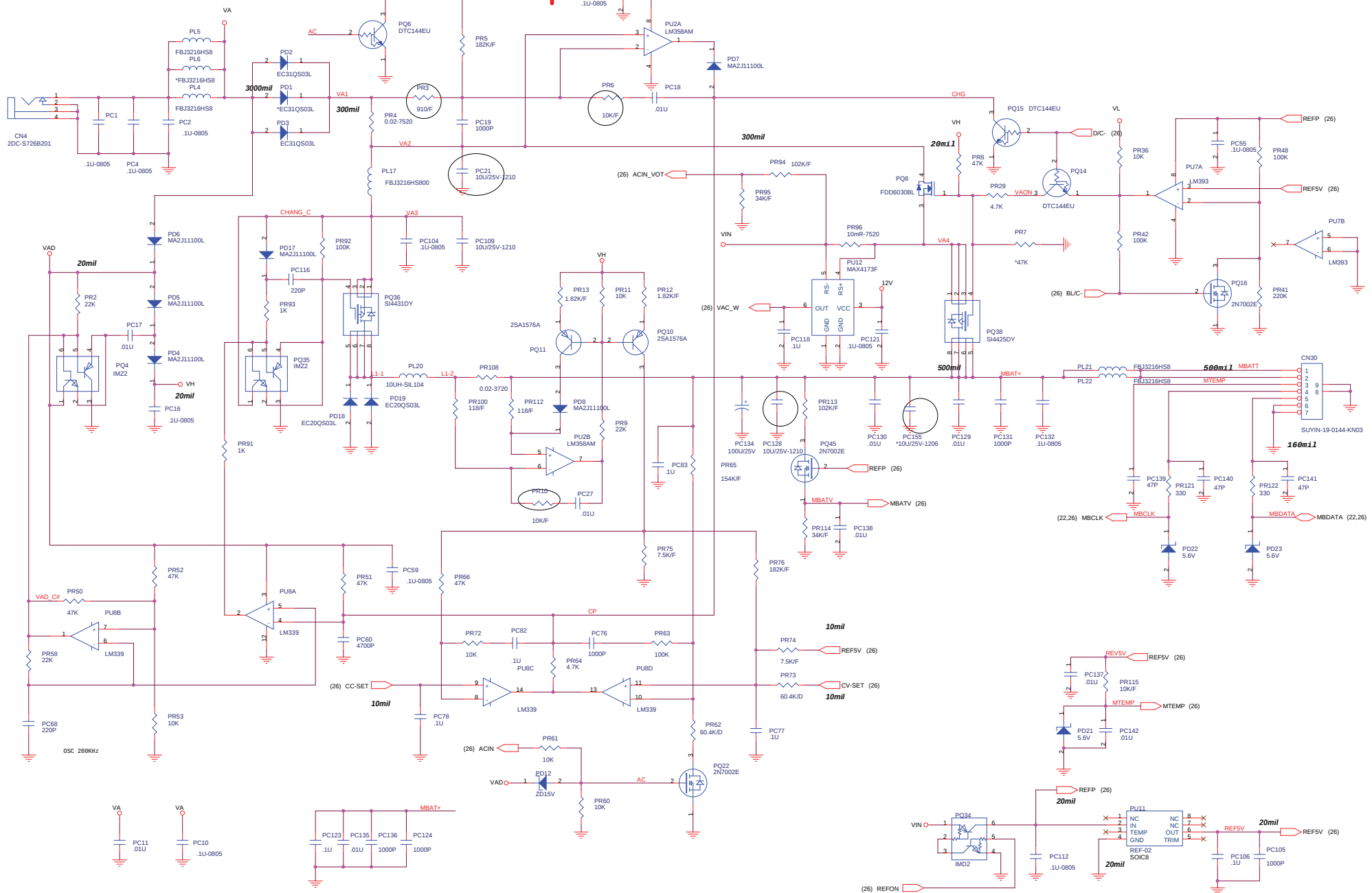


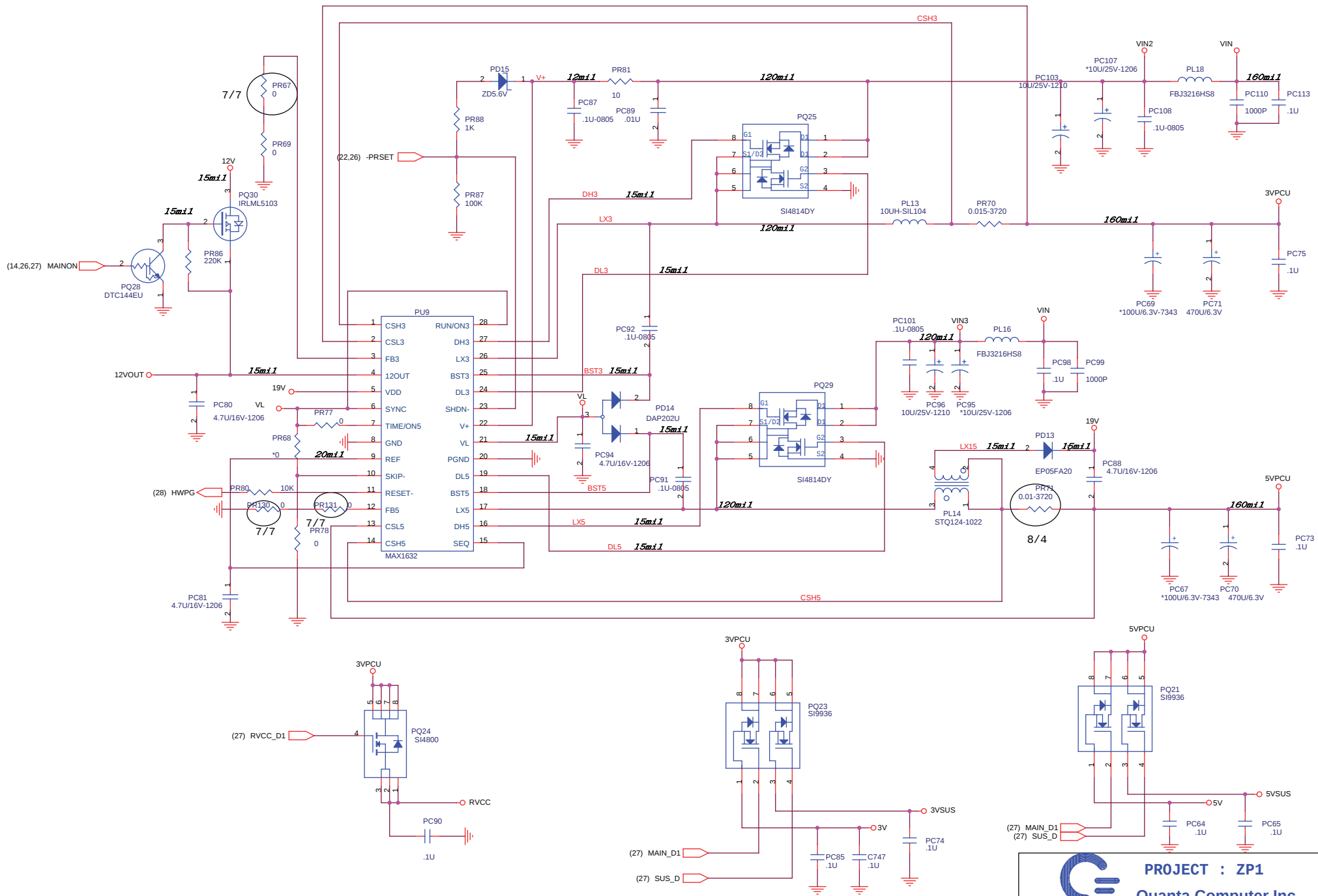
 PROJECT : ZP1 Qanta Computer Inc.		
Size A3	Document Number LAN PHY VT6103 + RJ11&RJ45, 570 EXP. IO	Rev 2A
Date:	Wednesday, September 17, 2003	Sheet 25 of 32

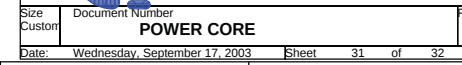
ITEM 85, Rev.B remove jumper



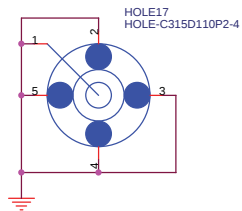
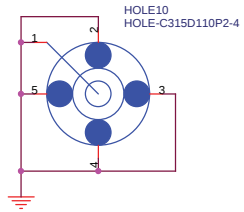
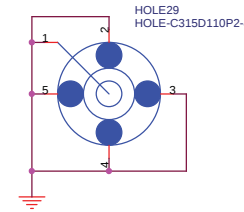
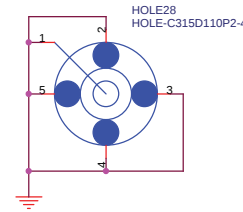
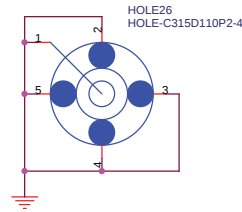
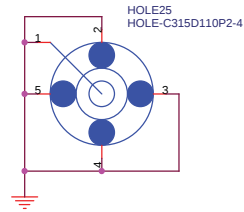
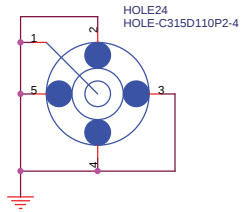
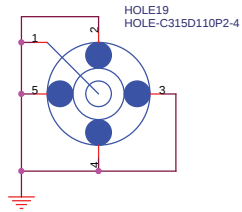
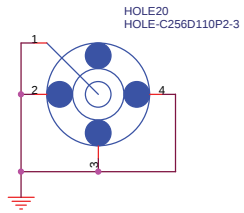
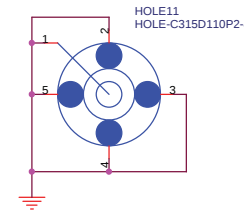
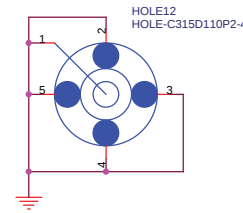
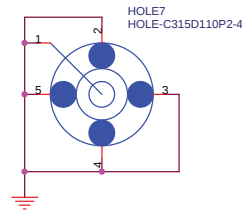
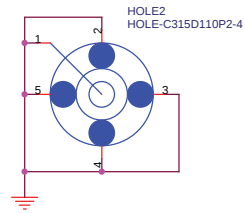
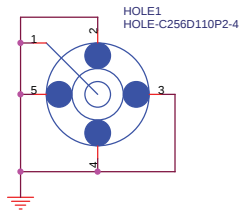
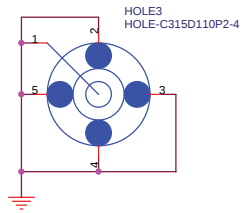




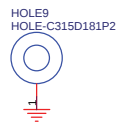
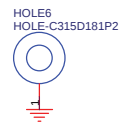
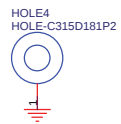




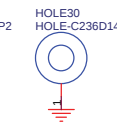
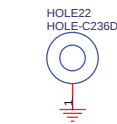
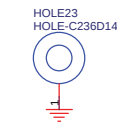
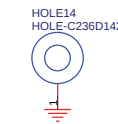
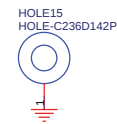
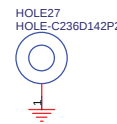
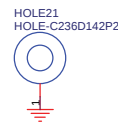
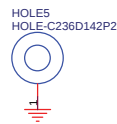
A



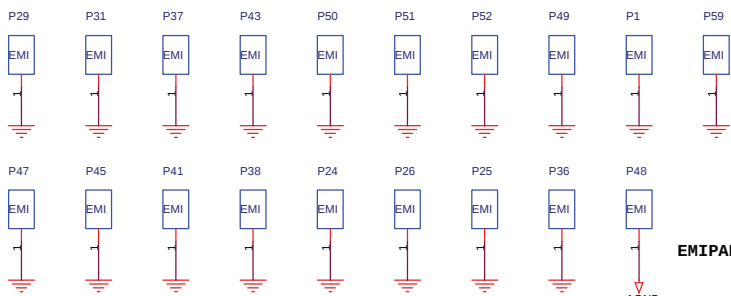
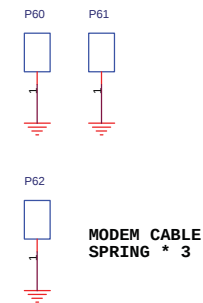
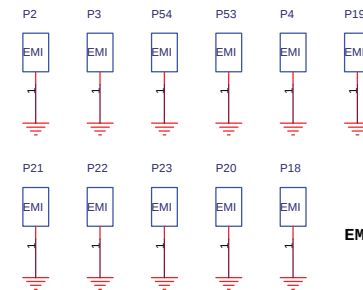
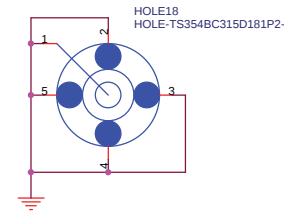
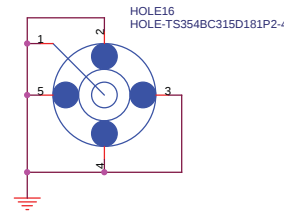
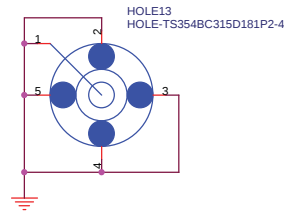
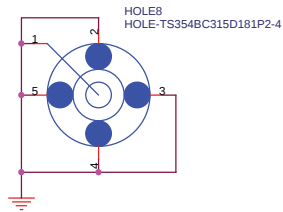
d



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AGND

